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A New High Gain DC-DC Converter for Solar System

Mohammad Sarvi[a*], Reza Ebrahimnaz[b], Homa Zarei Zohdi[a]

[a] *School of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran.*
[b] *Department of Electrical Engineering Imam Khomeini International University, Qazvin, Iran.*

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A B S T R A C T

Renewable energy, such as solar, is crucial to combating the environmental effects of fossil fuels. Some studies have proposed a step-up converter based on a conventional boost converter and a coupled inductor. This paper proposes a high step-up DC-DC converter designed for solar system applications. The interleaving method is used at the converter's input to reduce the input current ripple and increase the voltage gain. This converter has a high voltage gain and a low voltage stress on the semiconductor elements, while the conduction losses of the converter are reduced. The proposed converter with a power of 220 watts, an input voltage of 10 volts, and an output voltage of 120 volts is simulated in MATLAB software. Ultimately, the performance of the converter has been assessed through analysis and simulation. Furthermore, the converter's performance was compared with several similar topologies. The results and comparisons clearly demonstrate the effectiveness of the proposed converter.

1. Introduction

Studies in various fields focus on decreasing greenhouse gas emissions using renewable energy sources (RES) [1]. Solar photovoltaic (PV) energy is a renewable energy sources that provides an alternative to fossil fuels [2]. Power electronic converters are essential in photovoltaic systems, enabling efficient energy conversion for various applications [3]-[4]. The voltage generated by the solar cells is relatively low [5]-[6]. To increase voltage levels, solar cells are connected together in series, however, optimal power generation power generation requires the use of a boost converter [7]-[8]. The overall architecture of the solar system with a high-voltage gain converter is depicted in Figure 1.

*Corresponding Author Email:msarvi@iust.ac.ir

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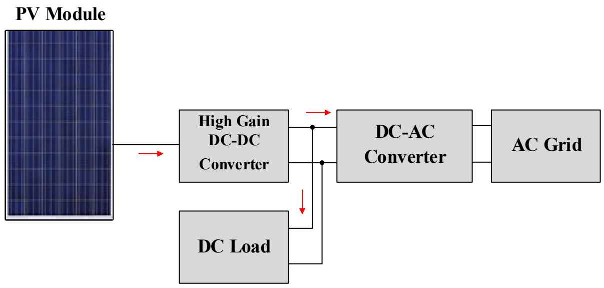


Figure 1. General architecture of PV system.

Boost converter topologies suffer from low voltage-gain issues; therefore, Khan et al. [9] have introduced an improved high-gain converter. High-gain non-isolated converters are typically applied in medium-power applications due to their low cost and high efficiency. Researchers have presented several topologies for high-gain converters, and evaluating the advantages and disadvantages of each have been examined [10]. The increasing demand for RES and energy storage systems has created new opportunities for innovation in DC-DC conversion technologies [11]. Ebrahimnaz and Sarvi [12] have investigated a step-up converter with minimal stress on semiconductor components for incorporation into photovoltaic systems. Padmanaban et al. [13] have presented a quasi-Z-source converter that utilizes an inductor and a switched-capacitor arrangement. Hajilou and Farzanehfard [14] have introduced a high-voltage gain converter based on a Z-quasi-source structure.

Forouzesh et al. [15] have suggested a non-isolated step-up converter with switching capacitors. Nabati et al. [16] have stated that the DC-DC converter provides a non-isolated boost for high-voltage applications but does not achieve a very high voltage gain. Najafi et al. [17] have presented a new converter topology with high voltage gain for solar system applications; however, the number of converter components is high. Naderi et al. [18] have presented a new topology of a boosted DC-DC converter, but they did not investigate the voltage stress on the switches. High-gain cascade converters have been comprehensively compared in the literature [19]-[20]-[21]. Some studies have proposed a step-up converter based on a conventional boost converter and a coupled inductor [22]-[23]. Shibu et al. [24] have introduced a converter with a high step-up for microgrid applications. Mejbel et al. [25] have developed a self-switched boost converter with low voltage gain. Previous studies have examined quadratic boost converters and outlined their advantages and disadvantages [26]-[27]. Ahmad et al. [28] have designed a converter for a solar system to increase the voltage gain using two switches.

In this paper, a high-gain converter is introduced, and the performance of the converter is investigated by analysis and simulation. The results of this study will be useful for increasing the efficiency of solar energy systems. The following are the highlights and novelty of the work:

- New High-Gain DC-DC Converter:

The proposed structure significantly increased the input-to-output voltage level, making it beneficial for applications such as solar power systems, where a higher output voltage is desired.

- Utilization of Interleaving Technique at the Input:

This technique has improved the overall performance and reliability of the converter by effectively reducing the current ripple.

- Implementation of Two Voltage Multipliers at the Output:

The inclusion of two output voltage multipliers has been employed to increase the gain.

- Low Voltage Stress on Semiconductors:

This feature ensures that the components used in the converter experience lower voltage levels compared to other designs, potentially leading to increased reliability and longevity of the semiconductors.

- Reduced Conduction Losses and Enhanced Efficiency:

In this design, conduction losses have been minimized, resulting in improved efficiency of the converter.

The next part of the article is as follows: Section 2 presents the topology of the converter. In Part 3, the converter is compared with some similar converters. The simulation results are shown in Part 4; finally, the discussion is presented in Section 5, and the conclusion is provided in Section 6.

2. The Proposed Converter Design and Operational Principles

Figure 2 depicted the circuit schematic of the converter. The proposed converter employs the interleaving method in the input section to reduce ripple in the current and the combination of two voltage multiplier cells (VMCs) in the output section to enhance the voltage gain.

The pulses applied to each of the existing switches have a phase difference of 180 degrees, the duty cycle is greater than 0.5, and the same duty cycle is applied to both switches. In a switching period, the converter has four operating modes, the circuit for each mode is illustrated in Figure 3 and the key waveforms of the converter are illustrated in Figure 4. It should be noted that, in the analyses conducted, all active and passive elements were regarded as ideal.

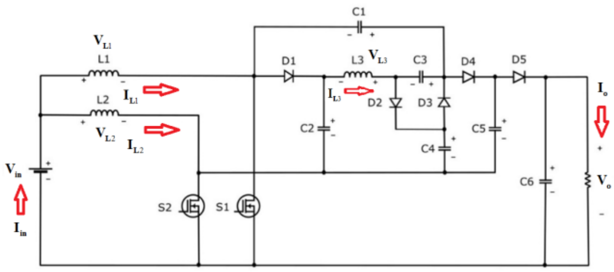


Figure 2. The suggested converter structure.

2.1. Operating Analysis

Mode 1 [t_0-t_1]: In this time duration, the switches S_1 and S_2 are on, and the energy does not transfer from the input to the output, and the output capacitor C_6 supplies power to the output load. The waveform of the converter in mode 1 is depicted in Figure 3(a). The relationships of this state are expressed as follows:

$$V_{L_1}=V_{L_2}=V_{in} \tag{1}$$

$$V_{L_3}=V_{C_1}-V_{C_2}-V_{C_3} \tag{2}$$

$$V_O=V_{C_6} \tag{3}$$

Mode 2 [t_1-t_2]a: Switch S_1 and diodes D_3 and D_5 are on, and switch S_2 and D_1, D_2, D_4, D_5 are off. In this mode, the inductor L_1 is charged, but the inductor L_2 starts to discharge when the switch S_2 turns off and transfers its energy to the output side of the circuit. The waveform of the converter in mode 2 can be depicted in Figure 3(b). The relationships of this state are expressed as follows:

$$V_{L_1}=V_{in} \tag{4}$$

$$V_{L_2}=V_{in}+V_{C_5}-V_O \tag{5}$$

$$V_{L_3}=V_{C_4}-V_{C_3}-V_{C_2} \tag{6}$$

Mode 3 [t_2-t_3]: This state is the same as mode 1 and the relations extracted for working mode 1 are also valid for this mode. This operating mode ends when switch S_1 turns off, and diodes D_1, D_2 and D_4 turn on. The converter's waveform in mode 3 is depicted in Figure 3(c).

Mode 4 [t_3-t_4]: In this state, switch S_2 and diodes D_1, D_2, and D_4 are on, while switch S_1 and D_3, D_5 are off. In this mode, the inductor L_1 is discharged and its energy is transferred to the output section. Because D_5 is off in this state, the output load is powered by the capacitor C_6. The waveform in mode ٤ is depicted in Figure 3(d). This is extracted as follows:

$$V_{L_1}=V_{in}-V_{C_2}=V_{in}+V_{C_1}-V_{C_5} \tag{7}$$

$$V_{L_2}=V_{in} \tag{8}$$

$$V_{L_3}=V_{C_4}-V_{C_2}=V_{C_1}-V_{C_3}=V_{C_5}-V_{C_3}-V_{C_2} \tag{9}$$

$$V_{C_5}=V_{C_3}+V_{C_4} \tag{10}$$

$$V_O=V_{C_6} \tag{11}$$

2.2. Calculate the voltage gain

Taking into consideration that the average voltage of an inductor is equal to zero in a switching period [12], and according to the relations obtained above, the voltages of the capacitors and the voltage gain are determined. First, the duration of each mode is as follows:

$$[t_0,t_1]=\frac{2D-1}{2}T \tag{12}$$

$$[t_2,t_3]=\frac{2D-1}{2}T \tag{13}$$

$$[t_1,t_2]=(1-D)T \tag{14}$$

$$[t_3,t_4]=(1-D)T \tag{15}$$

By setting the average voltage of inductors L_1 and L_2 to zero, the following relationships are obtained:

$$V_{C_2}=\frac{V_{in}}{1-D} \tag{16}$$

$$V_O-V_{C_5}=V_{C_1}-V_{C_4}=\frac{V_{in}}{1-D} \tag{17}$$

In mode 4:

$$V_{C_1} - V_{C_4} = V_{C_3} - V_{C_2} \tag{18}$$

By replacing equations (16) and (17) in (18):

$$V_{C_3} = \frac{2}{1\text{-}D} V_{in} \tag{19}$$

By simplifying equation (7) and inserting the calculated value for V_{C2}:

$$V_{C_5} - V_{C_1} = V_{C_2} = \frac{V_{in}}{1\text{-}D} \tag{20}$$

With zero consideration of the average voltage L_3:

$$DV_{C_1} + (1\text{-}D) V_{C_4} = \frac{D+2}{1\text{-}D} V_{in} \tag{21}$$

Using equations (17) and (21), the voltage values of capacitors C_1 and C_4 are obtained:

$$V_{C_1} = \frac{3}{1\text{-}D} V_{in} \tag{22}$$

$$V_{C_4} = \frac{2}{1\text{-}D} V_{in} \tag{23}$$

By replacing equations (19) and (23) in (10):

$$V_{C_5} = \frac{4}{1\text{-}D} V_{in} \tag{24}$$

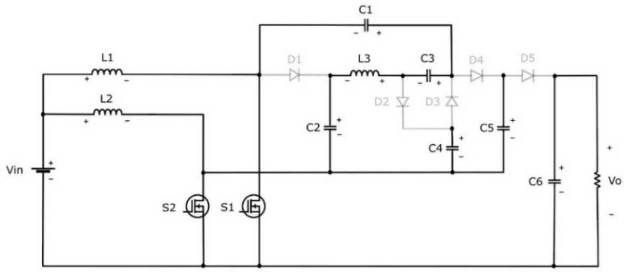
And finally, by inserting equation (24) into (17), the voltage gain is obtained:

$$M = \frac{V_O}{V_{in}} = \frac{5}{1\text{-}D} \tag{25}$$

The voltage gain curve as the duty cycle changes is illustrated in Figure 5.

2.3. Calculation of voltage stress of semiconductor elements

The voltages of switches and diodes are shown in Table 1 for all operating modes. According to Table 1, it is clear that the voltage stress on the semiconductors is lower than the V_o of the converter, and this feature allows for the use of components with a lower voltage range, which , as mentioned before, improves the efficiency.



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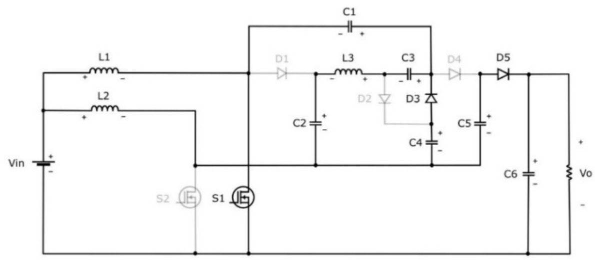

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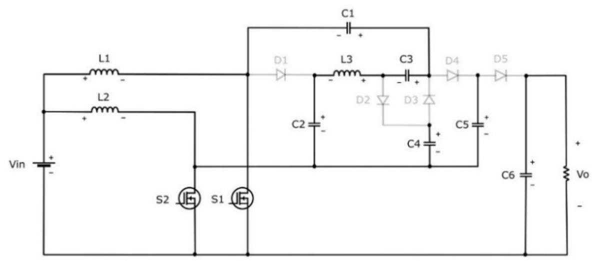

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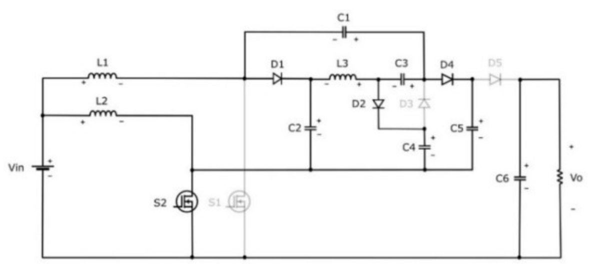


(d)

Figure 3. Modes of the converter. In state (a) 1, (b) 2, (c) 3, (d) 4.

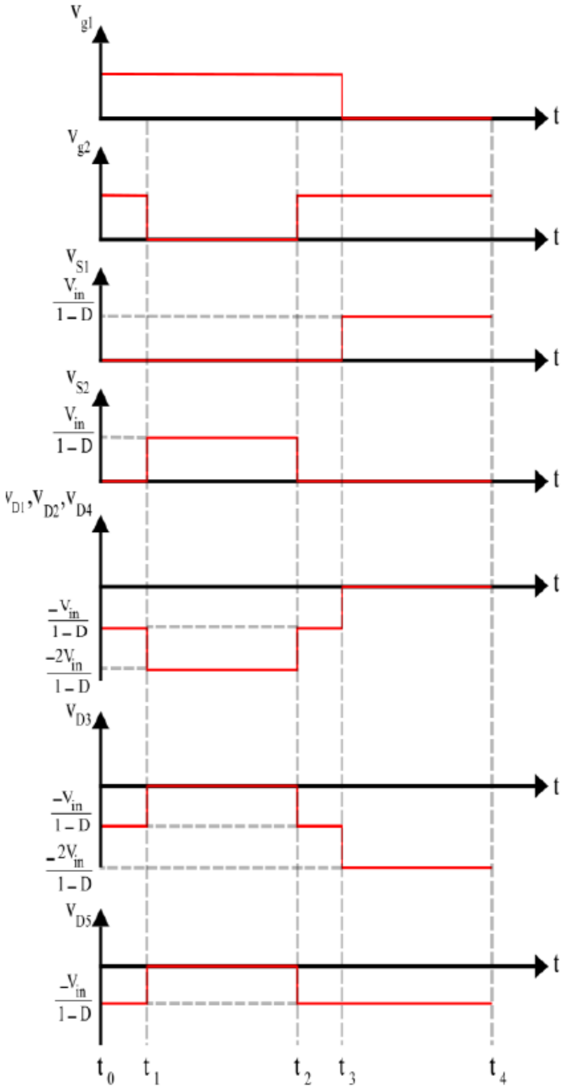


Figure 4. The waveforms of the converter

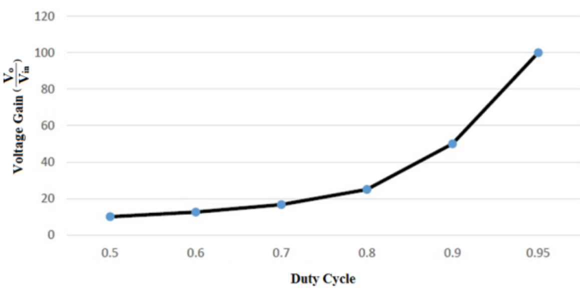


Figure 5. Converter voltage gain curve with respect to duty cycle changes

Table 1. Voltage stress of the semiconductor in the converter

	Mode1	Mode2	Mode3	Mode4
V_{S1}	0	0	0	$\frac{V_o}{5}$
V_{S2}	0	$\frac{V_o}{5}$	0	0
V_{D1}	$\frac{V_o}{5}$	$\frac{2}{5}V_o$	$\frac{V_o}{5}$	0
V_{D2}	$\frac{V_o}{5}$	$\frac{2}{5}V_o$	$\frac{V_o}{5}$	0
V_{D3}	$\frac{V_o}{5}$	0	$\frac{V_o}{5}$	$\frac{2}{5}V_o$

2.4. Design of input inductors

First, the values of I_{max} and I_{min}, the maximum and minimum of the currents of input inductors are defined according to Figure 6. The inductor current of L_1 in the first, second, and third operating states is determined by equation (26) [12]:

$$i_{L_1}(t)=\frac{I_{max}-I_{min}}{DT}t+i_{min} \tag{26}$$

The inductor current of L_2 in the second operating mode is defined by equation (27) [12]:

$$i_{L_2}(t)=\frac{I_{min}-I_{max}}{(1-D)T}(t-\frac{T}{2})+i_{min} \tag{27}$$

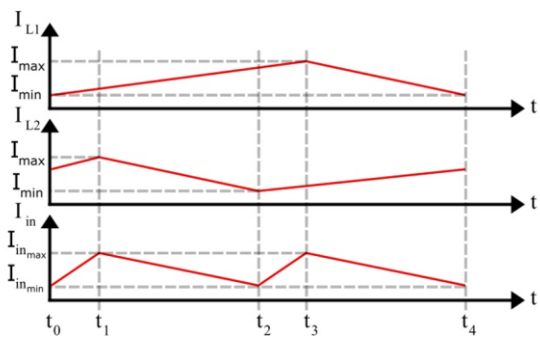


Figure 6. Current waveforms of input inductors

According to equation (28), the total input current is calculated as follows:

$$i_{in}=i_{L_1}+i_{L_2} \tag{28}$$

The current of the inductors at the beginning of the mode (at $t=\frac{2D-1}{2}T$) is equal to [12]:

$$i_{L_1}\left(t=\frac{2D-1}{2}T\right)=\frac{(i_{max}-i_{min})(2D-1)}{2D}+i_{min} \quad (29)$$

$$i_{L_2}\left(t=\frac{2D-1}{2}T\right)=i_{max} \quad (30)$$

The total input current is obtained at the beginning of the mode 2:

$$i_{in}\left(t=\frac{2D-1}{2}T\right)=i_{in_{max}}=\frac{i_{min}-i_{max}}{2D}+2i_{max} \quad (31)$$

The value of the current of the inductors at the end of state 2, (i.e. at) is equal to [6]:

$$i_{L_1}\left(t=\frac{T}{2}\right)=\frac{i_{max}-i_{min}}{2D}+i_{min} \quad (32)$$

$$i_{L_2}\left(t=\frac{T}{2}\right)=i_{min} \quad (33)$$

The amount of the total input current at the end of state 2 is obtained as equation (34):

$$i_{in}\left(t=\frac{T}{2}\right)=i_{in_{min}}=\frac{i_{max}-i_{min}}{2D}+2i_{min} \quad (34)$$

Using the ripple equations (31) and (34), the total input current is calculated:

$$\Delta i_{in}=i_{in_{max}}-i_{in_{min}}=2\left(i_{max}-i_{min}\right)+\frac{i_{min}-i_{max}}{D} \quad (35)$$

Also for inductor L_2 in the second operating mode [6]:

$$i_{L_2}\left(t=t_2\right)=i_{min}=\frac{1}{L_2}\left(\int_{t_1}^{t_2}\frac{-DV_{in}}{1-D}dt\right)+i_{max} \quad (36)$$

$$i_{max}-i_{min}=\frac{DTV_{in}}{L_2} \quad (37)$$

By replacing equation (37) in equation (35), the values of the inductors $\left(L_1=L_2=L\right)$ by assumption $(T=\frac{1}{f_s})$ are calculated as follows [6]:

$$\Delta i_{in}=\frac{(2D-1)V_{in}}{Lf_s} \quad (38)$$

$$L_1=L_2=L=\frac{(2D-1)V_{in}}{f_s\Delta i_{in}} \quad (39)$$

2.5. Capacitor design

In the converter, the diode D_5 is on only in the mode 2, and the capacitor C_6 is charged. In other modes, the capacitor C_6 is discharged.

Therefore, to calculate the output capacitor C_6, at first, operating modes 3 and 4 are considered [29].

$$V_C\left(t\right)=\frac{1}{C}\left(\int_{t_0}^{t_1}i_C\left(t\right)dt+\int_{t_2}^{t_3}i_C\left(t\right)dt+\int_{t_3}^{t_4}i_C\left(t\right)dt\right)+V_0(t) \quad (40)$$

The current of the capacitor C_6 in these three operating modes is equal to:

$$i_{C_6}=-I_O \quad (41)$$

Using the relationships above, the value of the output capacitor is obtained [29]:

$$C_O=\frac{DI_O}{f\Delta V_C} \quad (42)$$

According to equation (42), to reduce the output voltage ripple, the value of the output capacitor increased.

3. Performance Comparison

In this sector, the converter is compared with other interleaved boost converters that have a symmetrical or conventional structure. In Table 2, the converters are compared based on voltage stress, voltage gain, and the number of elements. In this comparison, the switch and the diode are selected, which exhibit the highest voltage stress. The comparison results indicate that the converter achieves a higher voltage gain relative to other converters without relying on coupling inductors or transformers by utilizing a unique combination of an interleaved input stage and dual voltage multiplier cells at the output.

4. Simulation Results

To further investigate the proposed converter, a 220-watt converter with an input voltage of 10 volts and an output voltage of 120 volts with the values and elements presented in Table 3 was simulated in MATLAB software, and the results are shown in Figures 7 to 11. Given that the simulation attempted to use real components, converter losses were also considered. Due to the consideration of losses, the simulation results differ somewhat from the ideal case. The voltage and current waveforms of switches S_1 and S_2 are shown in Figures 7 and 8, respectively. The current and voltage waveforms of diodes D_1 to D_5 are presented in Figure 9. According to Figure 10, the output voltage is 119.1 volts, and the total input current in Figure 11 is equal to 22 A.

The simulation results demonstrate that the suggested converter delivers a high voltage gain. This directly translates into higher efficiency and improved reliability, as the reduced stress allows the use of components with lower ratings, reducing both costs and potential failure rates.

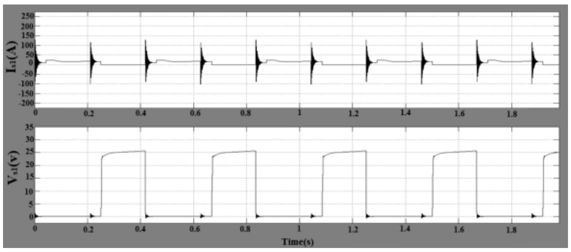


Figure 7. The waveform of switch S_1

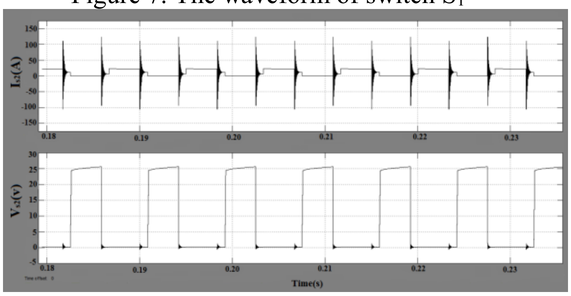
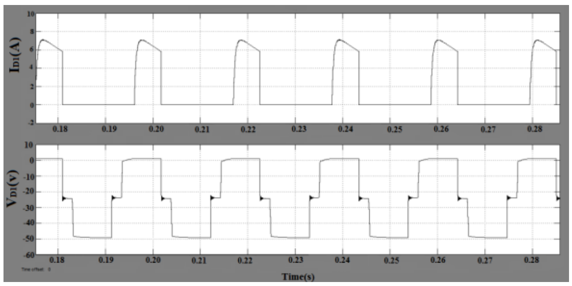


Figure 8. The waveform of switch S_2

Table 2. Comparison of the converter and the converters provided in the references

Topology	Proposed converter	Ref [29]	Ref[30]	Ref[31]	Ref[32]
Total number of components	19	23	14	34	13
Switches	2	2	2	6	3
Diodes	5	8	4	14	3
Capacitors	6	9	3	8	4
Inductors	3	4	2	6	3
Coupled inductors or built-in transformers	0	0	3	0	0
Number of magnetic cores	3	4	3	6	3
Voltage gain	$\frac{5}{1-D}$	$\frac{1+3D}{1-D}$	$\frac{2+n}{1-D}$	$\frac{3+D}{1-D}$	$\frac{\frac{8}{3}-3D}{(1-D)(\frac{2}{3}-D)}$
Voltage stress of switches	$\frac{V_o}{5}$	$\frac{V_O}{3+D}$	$\frac{V_O}{2+n}$	$\frac{V_O}{3+D}$	$\frac{1-D}{\frac{8}{3}-3D}V_O$
Maximum Voltage stress across diodes	$\frac{2}{5}V_o$	$\frac{DV_O}{1+3D}$	V_0	$\frac{2V_O}{3+D}$	$\frac{5-6D}{8-9D}V_O$



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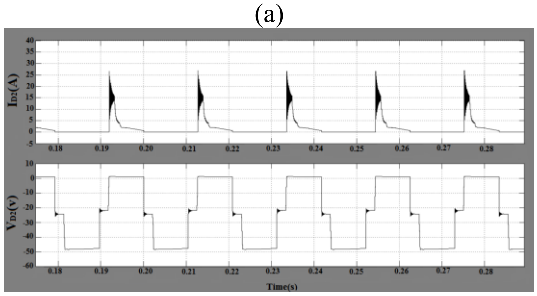

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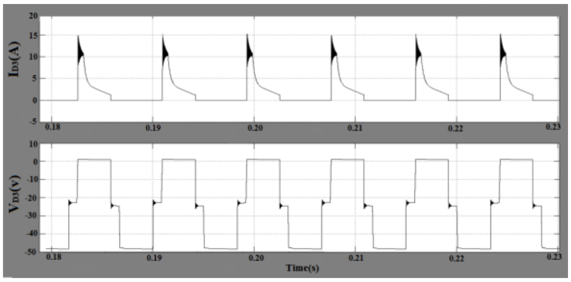

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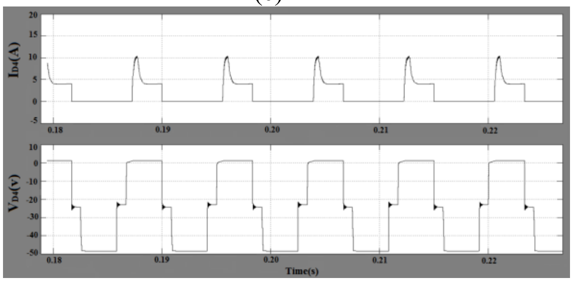

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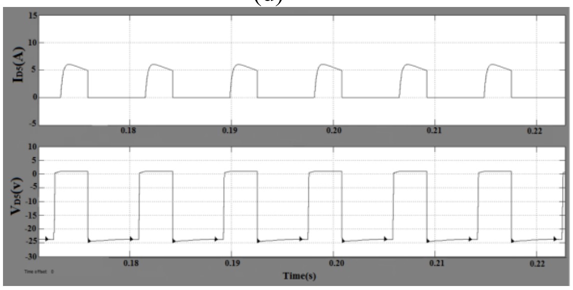

(e)

Figure 9. Current and voltage waveforms of diodes: (a) D_1, (b) D_2, (c) D_3, (d) D_4, (e) D_5.

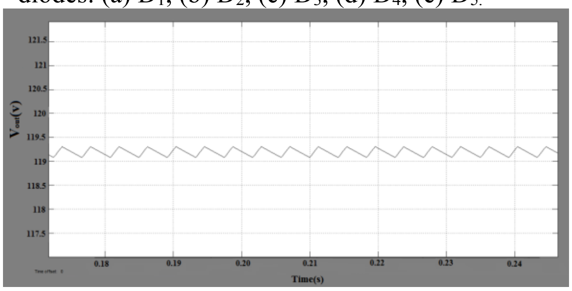

Figure 10. Output voltage waveform of the converter

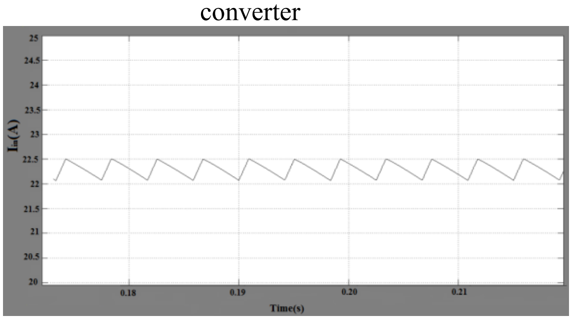

Figure 11. Input current waveform.

Table 3. Specifications of the converter in the simulation

Parameter	Value	Parameter	Value
V_{in}	10 V	C_4	100 μF
V_o	125 V	C_6	220 μF
P_{out}	200 W	L_1,L_2	200 μH
f_s	24 kHz	L_3	100 μH
C_1,C_5	150 μF	S_1,S_2	IPP110N20N3
C_2	100 μF	D_1-D_5	STTH15L06
C_3	47 μF	D (Duty cycle)	0.6

The converter's efficiency diagram for different output power (less than 220 watts) is shown in Figure 12.

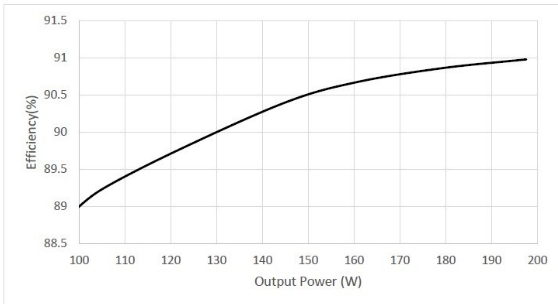

Figure 12. The efficiency curve of the converter with respect to the output load changes

5. Discussion

The simulation and analysis results demonstrate that the converter achieves a high voltage gain. This directly results in higher efficiency and enhanced reliability. The comparative analysis (as shown in Table 2) indicates that the proposed topology utilizes fewer components than traditional designs. This reduction in the number of components not only simplifies the overall design but also reduces manufacturing and maintenance costs, making the converter an attractive solution for cost-sensitive applications. The converter can be used for solar photovoltaic systems, distributed generation and renewable energy systems, microgrids, and battery storage systems. Future work on this converter includes investigating the converter's behavior under dynamic loading and varying environmental conditions, as well as integrating advanced maximum power point tracking (MPPT) algorithms with it.

6. Conclusions

The proposed converter achieves a notably high voltage gain which outperforms other similar converters while avoiding the use of coupling inductors and transformers. By incorporating an interleaved input stage and dual voltage multiplier cells, the design reduces input current ripple and minimizes voltage stress on semiconductor components, thereby enhancing overall efficiency and reliability. A comparative analysis demonstrates that our topology not only reduces the number of required components but also offers a cost-effective solution for high step-up conversion in low-voltage applications. The converter is particularly suited for solar applications, where low-voltage PV modules need to be efficiently stepped up to higher voltages for grid interfacing or energy storage.

Nomenclature

D	Duty cycle
f_s	Switching frequency (kHz)
I_{max}	Maximum current in the input inductors (Amp)
I_{min}	Minimum current in the input inductors (Amp)
i_{L1}	Inductor current of L_1 (Amp)
MPPT	Maximum power point tracking
PV	Photovoltaic
Pout	Output power (W)
RES	Renewable energy sources
V_o	Output voltage (V)
V_{in}	Input voltage (V)
V_{C1}	Voltage values of capacitors C_1 (V)
VMC	Voltage multiplier cell

References

[1] Sutikno T, Purnama HS, Widodo NS, Padmanaban S, Sahid MR. A review on non-isolated low-power DC–DC converter topologies with high output gain for solar photovoltaic system applications. Clean Energy 2022;6:557–72. DOI: 10.1093/ce/zkac037.

[2] Yang J, Lee H, Cho JS, Lim K, Kim H-C, Kim S, et al. A 5.5–276 W Integrated Photovoltaic Energy Harvesting System With 99.95% MPPT Efficiency and 98.74% Power Conversion Efficiency. IEEE Trans Power Electron 2025;40:4522–35.DOI: 10.1109/TPEL.2024.3508746.

[3] Jafari H, Vaez-Zadeh S. Investigation of a New Topology for Multilevel Inverters Fed by Photovoltaic System for Linear Induction Motor. J Sol Energy Res 2022;7. DOI: 10.22059/jser.2022.344742.1246.

[4] Zohdi HZ, Sarvi M. Analysis and Design of a New DC-DC Converter for DC Smart Grid. J Sol Energy Res 2023;8:1547–58. DOI: 10.22059/jser.2023.357223.1290.

[5] Hu X, Dai G, Wang L, Gong C. A Three-State Switching Boost Converter Mixed With Magnetic Coupling and Voltage Multiplier Techniques for High Gain Conversion. IEEE Trans Power Electron 2016;31:2991–3001. DOI: 10.1109/TPEL.2015.2453634.

[6] Wang YF, Xue LK, Wang CS, Wang P, Li W. Interleaved High-Conversion-Ratio Bidirectional DC-DC Converter for Distributed Energy-Storage Systems-Circuit Generation, Analysis, and Design. IEEE Trans Power Electron 2016;31:5547–61. DOI: 10.1109/TPEL.2015.2496274.

[7] Veerabhadra, Nagaraja Rao S. Assessment of high-gain quadratic boost converter with hybrid-based maximum power point tracking technique for solar photovoltaic systems. Clean Energy 2022;6:632–45. DOI: 10.1093/ce/zkac041.

[8] Upadhyay P, Kumar R. A high gain cascaded boost converter with reduced voltage stress for PV application. Sol Energy 2019;183:829–41. DOI: 10.1016/j.solener.2019.03.075.

[9] khan F, Zaid M, Tariq A, Khan MMA. A new non-isolated high-gain DC-DC converter for the PV application. E-Prime - Adv Electr Eng Electron Energy 2023;5. DOI: 10.1016/j.prime.2023.100198.

[10] Gu Y, Chen Y, Zhang B, Qiu D, Xie F. High Step-Up DC-DC Converter with Active Switched LC-Network for Photovoltaic Systems. IEEE Trans Energy Convers 2019;34:321–9. DOI: 10.1109/TEC.2018.2876725.

[11] Ai J, Lin M. Ultralarge Gain Step-Up Coupled-Inductor DC-DC Converter with an Asymmetric Voltage Multiplier Network for a Sustainable Energy System. IEEE Trans Power Electron 2017;32:6896–903. DOI: 10.1109/TPEL.2016.2626383.

[12] Ebrahimnaz R, Sarvi M. A Novel Interleaved DC-DC Converter with High Voltage Gain for Photovoltaic System Applications. J Sol Energy Res 2022;7:1056–66. DOI: 10.22059/jser.2022.330278.1220.

[13] Padmanaban S, Maroti PK, Holm-Nielsen JB, Blaabjerg F, Leonowicz Z, Yaramasu V. Quazi Z-Source Single Stage High Step-Up DC-DC

Converter for Grid-connected PV Application. Proc. - 2019 IEEE Int. Conf. Environ. Electr. Eng. 2019 IEEE Ind. Commer. Power Syst. Eur. EEEIC/I CPS Eur. 2019, 2019. DOI: 10.1109/EEEIC.2019.8783239.
[14] Hajilou M, Farzanehfard H. Fully Soft-Switched High Voltage Gain Quasi-Z-source Converter With Continuous Input Current and Low Switch Voltage Stress. IEEE Trans Power Electron 2025:1–9. DOI: 10.1109/TPEL.2025.3529634.
[15] Forouzesh M, Siwakoti YP, Gorji SA, Blaabjerg F, Lehman B. Step-Up DC-DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications. IEEE Trans Power Electron 2017;32:9143–78. DOI: 10.1109/TPEL.2017.2652318.
[16] Yaser Nabati , Abolfazl Halvaei Niaser hamidreza mohammadi. A New L-C-D Cell Based Non-Isolated Single Switch High Step-Up DC-DC Converter for Photovoltaic Applications. J Sol Energy Res 2022;7:1027–36. DOI: 10.22059/jser.2022.332911.1226.
[17] Najafi E, Shojaeian H, Kashi M. A high gain Step up converter for solar applications based on PSOL topology. J Sol Energy Res 2019;4:180–7. DOI: 10.22059/jser.2019.283409.1116.
[18] Naderi E, SeyedShenava SJ, Shayeghi H. High Gain DC/DC Converter Implemented with MPPT Algorithm for DC Microgrid System . J Oper Autom Power Eng 2023;11:213–22. DOI: 10.22098/joape.2023.10270.1731.
[19] Murad Z, Anzi F Al, Ben-Brahim L. A Comparative Study of High-gain Cascaded DC-DC Converter Topologies. 2022 3rd Int. Conf. Smart Grid Renew. Energy, IEEE; 2022, p. 1–6. DOI: 10.1109/SGRE53517.2022.9774048.
[20] Sharma P, Hasanpour S, Kumar R. Advancing renewable energy: A quadratic high-efficiency high gain step-up DC/DC converter. E-Prime - Adv Electr Eng Electron Energy 2024;10:100847. DOI: 10.1016/j.prime.2024.100847.
[21] Zhang S, Li H, Duan S, Du X, Liu S, Wang P, et al. A High-Gain DC-DC Converter with a Wide Range of Output Voltage. Electronics 2023;12:3498. DOI: 10.3390/electronics12163498.
[22] Karimi Hajiabadi M, Mosallanejad A, Salemnia A. Ultra- high gain quadratic boost DC–DC converter based on a three- winding coupled inductor with reduced voltage stress for fuel cell- based systems. IET Power Electron 2023;16:2666–81. DOI: 10.1049/pel2.12592.
[23] Fan X, Sun H, Yuan Z, Li Z, Shi R, Ghadimi N. High Voltage Gain DC/DC Converter Using Coupled Inductor and VM Techniques. IEEE Access 2020;8:131975–87. DOI: 10.1109/ACCESS.2020.3002902.
[24] Shibu S, Babu E, Neema S, Joy N. High gain DC-DC converter with low voltage stress. Mater Today Proc 2022;58:600–6. DOI: 10.1016/j.matpr.2022.04.027.
[25] Mejbel IA, Hassan TK. DESIGN AND SIMULATION OF HIGH GAIN SEPIC DC–DC CONVERTER. J Eng Sustain Dev 2023;27:138–48. DOI: 10.31272/jeasd.27.1.12.
[26] Moradisizkoohi H, Elsayad N, Mohammed O. A soft-switched dc/dc converter using integrated dual half-bridge with high voltage gain and low voltage stress for dc microgrid applications. Inventions 2018;3. DOI: 10.3390/inventions3030063.
[27] Kumar M, Panda KP, Naayagi RT, Thakur R, Panda G. A Critical Analysis of Quadratic Boost Based High-Gain Converters for Electric Vehicle Applications: A Review. Sensors 2024;24:2186. DOI: 10.3390/s24072186.
[28] Ahmad J, Siddique MD, Sarwar A, Lin CH, Iqbal A. A high gain noninverting DC–DC converter with low voltage stress for industrial applications. Int J Circuit Theory Appl 2021;49:4212–30. DOI: 10.1002/cta.3129.
[29] Ye H, Jin G, Fei W, Ghadimi N. High step-up interleaved dc/dc converter with high efficiency. Energy Sources, Part A Recover Util Environ Eff 2020:1–20. DOI: 10.1080/15567036.2020.1716111.
[30] Tseng K-C, Cheng C-A, Chen C-T. High Step-Up Interleaved Boost Converter for Distributed Generation Using Renewable and Alternative Power Sources. IEEE J Emerg Sel Top Power Electron 2017;5:713–22. DOI: 10.1109/JESTPE.2016.2611641.
[31] Maalandish M, Hosseini SH, Ghasemzadeh S, Babaei E, Shalchi Alishah R, Jalilzadeh T. Six- phase interleaved boost dc/dc converter with high- voltage gain and reduced voltage stress. IET Power Electron 2017;10:1904–14. DOI: 10.1049/iet-pel.2016.1029.
[32] Saadatizadeh Z, Heris PC, Sabahi M, Babaei E. A DC–DC Transformerless High Voltage Gain Converter With Low Voltage Stresses on Switches and Diodes. IEEE Trans Power Electron 2019;34:10600–9. DOI: 10.1109/TPEL.2019.2900212.