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A Multilevel Inverter Structure Based on the Development of Full-Bridge Cells with the Minimum Number of Switches for Renewable Energy Applications

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Abstract

Because of the rise in electricity consumption, renewable energy sources such as the solar and wind are increasingly being used to generate electricity. The integration of renewable energy sources into the grid is critical to energy utilization. The major goal of the new proposed structures is to achieve high output voltage while using fewer power electronic elements such as switches, diodes, and DC input voltage sources, unlike conventional topologies. In addition to lowering costs, size, and complexity, reducing the number of switches and DC voltage sources improves inverter performance. This paper presents a general multilevel inverter based on full-bridge cells. Two specific cases of proposed topology are investigated in detail. The proposed structures have the advantage of reducing the power electronic elements and the switching complexity. It is also possible to configure asymmetric sources to achieve maximum output levels. The first special case is a synthesis with seventeen levels of output, four input voltage sources, and nine switches achieved to the Total Harmonic Distortion (THD) of output voltage equal to 5.68% in 100 HZ frequency of switching carriers and THD of output voltage equal to 6.69% for 5000 HZ frequency of switching carriers. The second case involves the synthesis of forty-three levels of output with six input voltage sources and twelve switches achieved to the THD of output voltage equal to 3.49% in 100 HZ frequency of switching carriers and THD of output voltage 3.99% for 5000 HZ frequency of switching carriers. The proposed topologies are switched using a multicarrier pulse width modulation method. When compared to conventional structures, two special cases of this general topology have significantly reduced the number of power electronic switches. Also, a comparison of the proposed topology with the other structures, results show that the proposed structure has optimally reduced the number of power elements.

Keywords: Multilevel Inverter; Full Bridge; Renewable energy

1. Introduction

Today, DC/AC power conversion is critical in the generation, transmission, distribution, and utilization of electric power [1]. Multilevel inverters (MLI) play an important role in a variety of applications such as power supplies, flexible AC transmission systems, electric and hybrid electric vehicles, and the integration and utilization of renewable energy [2-16]. MLI is widely used in high and medium voltage conversion due to its high quality, low total harmonic distortion (THD), less stress on the switches, electromagnetic compatibility, and low switching losses.

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Many researchers have devoted their efforts in recent years to developing topologies for multilevel inverters. The 'Cascaded Half-Bridge based on multilevel DC link (MLDC)' is a multilevel inverter introduced in [17]. The structure is simple and highly modular, but isolated input DC levels are required. In [18-22], a competitive multilevel inverter topology was introduced in comparison to the classical topology. The topology is known as a 'packed U-cell' topology. It has a simple structure, but the sources must be asymmetric and isolated. [23] presents a multilevel inverter topology capable of accessing any combination of input sources. This topology necessitates the use of both unidirectional and bidirectional switches. The modular structure of the [23] topology is introduced in [24]. [25] describes a modular topology that can use both symmetric and asymmetric source configurations.

This paper presents a general multilevel inverter based on full-bridge cells. The proposed structures have the advantage of reducing the power electronic elements and the switching complexity. It is also possible to configure asymmetric sources to achieve maximum output levels. The innovation of this article is that we have achieved high voltage and current output levels compared to other similar structures by using the least switching elements and also by applying a suitable source pattern. The advantages of this paper structures are as follows: firstly, it eliminates the need to use an output filter, and secondly, it significantly reduces the number of power electronics elements compared to similar models that can produce the number of output surfaces of our structure .In fact, the main purpose of this topology is to reduce the number of power switches, reduce the complexity of using asymmetric resources, and reduce the complexity of switching.

The method of work has been that we have achieved the mentioned goals by using an innovative arrangement of power switches and voltage sources. The simulation results also show that by using the presented topology, both the number of power switches used has been reduced and the characteristic of betting and output current has been improved, which eliminates the need to use an output filter.

The following is how the paper is organized. Section 2 presents the proposed multilevel inverter with asymmetric source configuration. Section 3 discusses the simulation results for two special cases of the proposed topology. Section 4 contains the conclusion.

2. The proposed multilevel inverter topology

In this paper, a general multilevel inverter topology is presented, which can be simplified in a variety of ways. The structure of this topology is derived from the longitudinal and transverse expansion of the full bridge inverter cell. All "expansion" cells must be connected in such a way that there are always two common keys between the cell and the next extended cell, in both the transverse and longitudinal directions. Figure 1 depicts a full bridge inverter cell. This figure depicts the orientation of the cell's longitudinal and transverse extensions in order to achieve the proposed topology. Figure 1 also shows the general mode of the inverter's topology.

2-1 A review of two particular states of the proposed topology

The first special case of the proposed topology results from a longitudinal extension and two transverse extensions of the full bridge cell, resulting in a topology with four full bridge cells. Structure 1 is the name we give to this topology. The second special case of the topology is derived from two longitudinal extensions and three transverse extensions of the full bridge cell, resulting in a structure of six full bridge cells. Structure 2 is the name we give to this topology. The first special case is shown in Figure 2 a., and the second in Figure 2 b. demonstrates the proposed topology's second special case.

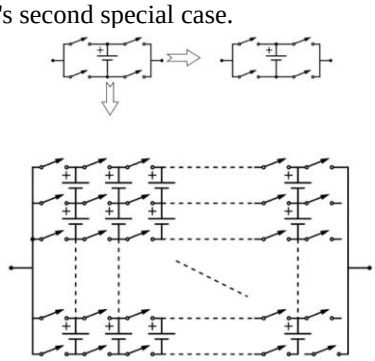


Figure 1: The longitudinal and transverse directions of the full bridge inverter cell to achieve the proposed topology.

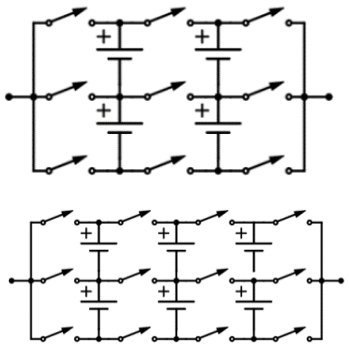


Figure 2: (a) The proposed topology's first special case, (b) The proposed topology's second special case.

To count the output voltage states of structure 1 consider Fig. 3 with V_1, V_2, V_3 and V_4 sources and $S_i\{i = 1\ to\ 9\}$ switches. Output voltage of inverter is V_{out}.

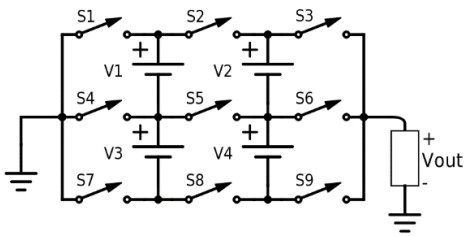


Figure 3: Topology of structure 1.

At first glance, the number of possible source combinations in the output appears to be the sum of 0, 1, 2, 3, and 4 options. This summation is depicted in Equation 1. However, due to the nature of the topology, some source combinations may not be synthesized, and it is possible that in some resource combinations, in addition to positive polarity, the negative polarity of that state can also be achieved.

At first glance, the number of possible source combinations in the output appears to be the sum of 0, 1, 2, 3, and 4 options. This summation is depicted in Equation 1. However, due to the nature of the topology, some source combinations may not be synthesized, and it is possible that in some resource combinations, in addition to positive polarity, the negative polarity of that state can also be achieved.

$$\binom{4}{0} + \binom{4}{1} + \binom{4}{2} + \binom{4}{3} + \binom{4}{4} \quad (1)$$

For topology in Fig. 3, the combination of one source is also possible for both positive and negative polarities, so the number of states is $2\binom{4}{1}$. For the binary combination of sources, we have $\binom{4}{2} = 6$ states, among these states $(V_1 - V_2)$, $(V_1 + V_3)$, $(V_3 - V_4)$ and $(V_3 + V_4)$ in addition to the positive polarities the negative polarities are also obtainable, so the total number of binary source combinations of resources is as following:

$$\binom{4}{2} - 4 + 2 \times 4 = 10 \quad (2)$$

The number of trinary combinations of sources is the same $\binom{4}{3} = 4$. Both positive and negative polarities in quaternary combinations of sources are obtainable, so the number of total states is equal to $2\binom{4}{4} = 2$. The selection of none source that is related to zero-level synthesis is also possible in three ways. Therefore, the number of combinations of topology sources in Figure 3 is equal to equation 3.

$$3\binom{4}{0} + 2\binom{4}{1} + \binom{4}{2} - 4 + 2 \times 4 + \binom{4}{3} + 2\binom{4}{4} = 27 \quad (3)$$

Table 1 shows various combinations of Fig. 3 sources and on switches for each state.

To count the output voltage states of structure 2 consider Fig. 4 with V_1, V_2, V_3, V_4, V_5 and V_6 sources and $S_i\{i = 1\ to\ 9\}$ switches. Output voltage of inverter is V_{out}.

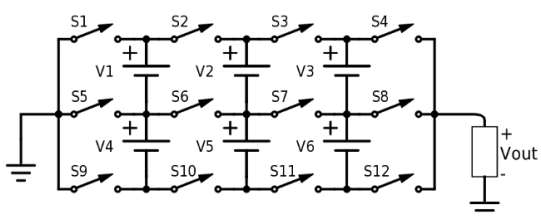


Figure 4: Topology of structure 2.

Table 1: Resource combinations states of structure 1 (topology of Fig 3).

State	ON switches	V_{out}
1	S_4, S_2, S_3	$+V_1$
2	S_1, S_5, S_6	$-V_1$
3	S_4, S_5, S_3	$+V_2$
4	S_1, S_2, S_6	$-V_2$
5	S_7, S_5, S_6	$+V_3$
6	S_4, S_8, S_9	$-V_3$
7	S_7, S_8, S_6	$+V_4$
8	S_4, S_5, S_9	$-V_4$
9	S_4, S_2, S_6	V_1-V_2
10	S_1, S_5, S_3	$-V_1+V_2$
11	S_7, S_5, S_9	V_3-V_4
12	S_4, S_8, S_6	$-V_3+V_4$
13	S_7, S_2, S_3	V_1+V_3
14	S_1, S_8, S_9	$-V_1-V_3$
15	S_7, S_8, S_3	V_2+V_4
16	S_1, S_2, S_9	$-V_2-V_4$
17	S_7, S_5, S_3	V_2+V_3
18	S_1, S_5, S_9	$-V_1-V_4$
19	S_7, S_2, S_6	$V_1+V_3-V_2$
20	S_1, S_8, S_9	$-V_1-V_3+V_4$
21	S_4, S_8, S_3	$V_2+V_4-V_3$
22	S_4, S_2, S_9	$-V_2-V_4+V_1$
23	S_7, S_2, S_9	$V_3+V_1-V_2-V_4$
24	S_1, S_8, S_3	$-V_1-V_3+V_4+V_2$
25	S_1, S_2, S_3	0
26	S_4, S_5, S_6	0
27	S_7, S_8, S_9	0

Same as structure 1, number of possible combinations of sources in the output is the summation of 0, 1, 2, 3, 4, 5 and 6 choices (equation 4), but due to the nature of the topology some of source combinations may not be synthesized and some of them may be achieved in both polarities. Total number of possible combinations of sources of Fig. 4 has shown in equation 5.

$$\binom{6}{0}+\binom{6}{1}+\binom{6}{2}+\binom{6}{3}+\binom{6}{4}+\binom{6}{5}+\binom{6}{6} \quad (4)$$

$$3\binom{6}{0}+2\binom{6}{1}+\binom{6}{2}-9+2\times 9+\binom{6}{3}-2-2+2\times 2+\binom{6}{4}-2-3+2\times 3+\binom{6}{5}-2+2\binom{6}{6}=81 \quad (5)$$

Different combinations of sources of structure 2 and on switches for each state are shown in table 2.

2-2 Provide an algorithm for asymmetric source configuration

Two or more of the MLI input sources have unequal values in an asymmetric source configuration. Utilization of asymmetric sources configuration has increased in recent years. Binary and trinary configurations are the most common arrangement of input sources. Consider multilevel inverter topology of Fig. 3. To obtain the highest number of output voltages possible, the voltages V_1, V_2, V_3 and V_4 are selected as follows:

$$V_1 = V_3 = V_{dc} \quad (6)$$

$$V_2 = V_4 = 4V_{dc} \quad (7)$$

According to equations 6 and 7, if the voltages of the sources V_1 and V_3 are four times the V_2 and V_4, then, according to table 1, a 17-level output with equal step is obtained. The multilevel inverter's various operating modes, Fig. 3, Figure 5 depicts the output voltage and switching arrangement, as well as the corresponding output voltage and switching arrangement.

Consider multilevel inverter topology of Fig. 4. To obtain the highest number of output voltages possible, the voltages V_1, V_2, V_3, V_4, V_5 and V_6 are selected as follows:

$$V_1 = V_4 = V_{dc} \quad (8)$$

$$V_2 = V_5 = 4V_{dc} \quad (9)$$

$$V_3 = V_6 = 5.5V_{dc} \quad (10)$$

If, according to the equations 8, 9 and 10, the V_1 and V_4 voltages are equal to V_{dc}, the V_2 and V_5 voltages are four times the V_{dc} and the voltages V_3 and $V_6$are considered five and a half times the V_{dc}, then according to table 2, a 41 level output with equal step and a 43 level output with two uneven levels at the beginning and the end are obtained. Part of the different operating modes of the multilevel inverter (structure 2), Figure 6 depicts the output voltage in conjunction with the output voltage.

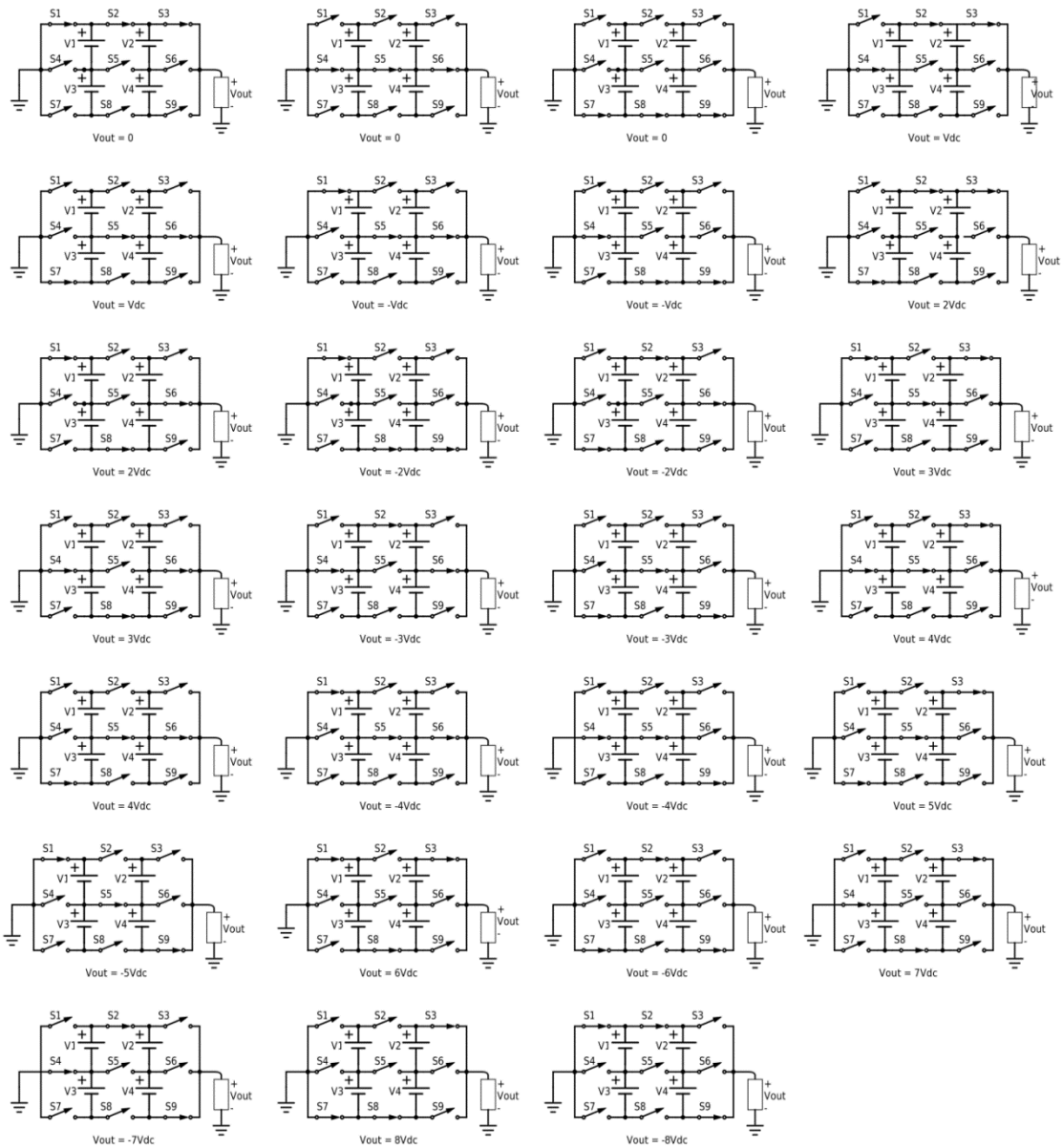


Figure 5:Various operating modes of the multilevel inverter (Fig. 3) with the corresponding output voltage and switching arrangement.

Table 2: Resource combinations states of structure 2 (topology of Fig 4).

State	ON switches	V_{out}	State	ON switches	V_{out}
1	S_2, S_5, S_3, S_4	$+V_1$	42	S_1, S_2, S_7, S_4	$-V_2 + V_3$
2	S_6, S_1, S_7, S_8	$-V_1$	43	S_9, S_6, S_3, S_4	$V_2 + V_4$
3	S_5, S_6, S_3, S_4	$+V_2$	44	S_9, S_{10}, S_3, S_4	$V_2 + V_5$
4	S_1, S_2, S_7, S_8	$-V_2$	45	S_1, S_2, S_{11}, S_{12}	$-V_2 - V_5$
5	S_5, S_6, S_4, S_7	$+V_3$	46	S_1, S_2, S_7, S_{12}	$-V_2 - V_6$
6	S_1, S_2, S_3, S_8	$-V_3$	47	S_9, S_6, S_7, S_4	$V_3 + V_4$
7	S_9, S_6, S_7, S_8	$+V_4$	48	S_9, S_{10}, S_7, S_4	$V_3 + V_5$
8	$S_5, S_{10}, S_{11}, S_{12}$	$-V_4$	49	S_9, S_{10}, S_{11}, S_4	$V_3 + V_6$
9	S_7, S_{10}, S_9, S_8	$+V_5$	50	S_1, S_2, S_3, S_{12}	$-V_3 - V_6$
10	S_5, S_6, S_{11}, S_{12}	$-V_5$	51	S_9, S_6, S_{11}, S_{12}	$V_4 - V_5$
11	S_9, S_{10}, S_{11}, S_8	$+V_6$	52	S_5, S_{10}, S_7, S_8	$-V_4 + V_5$
12	S_5, S_6, S_7, S_{12}	$-V_6$	53	S_9, S_6, S_7, S_{12}	$V_4 - V_6$
13	S_5, S_2, S_7, S_8	$V_1 - V_2$	54	S_5, S_{10}, S_{11}, S_8	$-V_4 + V_6$
14	S_1, S_6, S_3, S_4	$-V_1 + V_2$	55	S_9, S_{10}, S_7, S_{12}	$V_5 - V_6$
15	S_5, S_2, S_3, S_8	$V_1 - V_3$	56	S_5, S_6, S_{11}, S_8	$-V_5 + V_6$
16	S_1, S_6, S_7, S_4	$-V_1 + V_3$	57	S_5, S_2, S_7, S_4	$V_1 - V_2 + V_3$
17	S_9, S_2, S_3, S_4	$V_1 + V_4$	58	S_1, S_6, S_3, S_8	$-V_1 + V_2 - V_3$
18	$S_1, S_{10}, S_{11}, S_{12}$	$-V_1 - V_4$	59	S_9, S_2, S_7, S_8	$V_1 + V_4 - V_2$
19	S_1, S_6, S_{11}, S_{12}	$-V_1 - V_5$	60	S_5, S_2, S_{11}, S_{12}	$V_1 - V_2 - V_5$
20	S_1, S_6, S_7, S_{12}	$-V_1 - V_6$	61	S_5, S_2, S_7, S_{12}	$V_1 - V_2 - V_6$
21	S_5, S_6, S_3, S_8	$V_2 - V_3$	62	S_9, S_2, S_3, S_8	$V_1 + V_4 - V_3$
22	S_5, S_2, S_3, S_{12}	$V_1 - V_3 - V_6$	63	S_1, S_{10}, S_7, S_4	$-V_1 - V_4 + V_5 + V_3$
23	S_1, S_{10}, S_7, S_8	$-V_1 - V_4 + V_5$	64	S_9, S_2, S_3, S_{12}	$V_1 + V_4 - V_3 - V_6$
24	S_1, S_{10}, S_{11}, S_8	$-V_1 - V_4 + V_6$	65	S_1, S_{10}, S_{11}, S_4	$-V_1 - V_4 + V_3 + V_6$
25	S_1, S_6, S_{11}, S_8	$-V_1 - V_5 + V_6$	66	S_1, S_6, S_{11}, S_4	$-V_1 - V_5 + V_6 + V_3$
26	S_9, S_6, S_3, S_8	$V_2 + V_4 - V_3$	67	S_1, S_{10}, S_7, S_{12}	$-V_1 - V_4 + V_5 - V_6$
27	S_9, S_{10}, S_3, S_8	$V_2 + V_5 - V_3$	68	S_5, S_{10}, S_3, S_8	$-V_4 + V_5 + V_2 - V_3$
28	S_5, S_6, S_3, S_{12}	$V_2 - V_3 - V_6$	69	S_9, S_{10}, S_3, S_{12}	$V_2 + V_5 - V_3 - V_6$
29	S_5, S_{10}, S_3, S_4	$V_2 + V_5 - V_4$	70	S_1, S_2, S_{11}, S_4	$-V_2 - V_5 + V_3 + V_6$
30	S_1, S_2, S_{11}, S_8	$-V_2 - V_5 + V_6$	71	S_9, S_6, S_3, S_{12}	$V_4 + V_2 - V_3 - V_6$
31	S_5, S_{10}, S_7, S_4	$V_3 + V_5 - V_4$	72	S_5, S_{10}, S_{11}, S_4	$V_4 - V_5 + V_6 + V_3$
32	S_5, S_{10}, S_{11}, S_4	$V_3 + V_6 - V_4$	73	S_1, S_{10}, S_3, S_8	$-V_1 - V_4 + V_5 + V_2 - V_3$
33	S_5, S_6, S_{11}, S_4	$V_3 + V_6 - V_5$	74	S_5, S_2, S_{11}, S_4	$V_3 + V_6 - V_5 - V_2 + V_1$
34	S_9, S_6, S_{11}, S_8	$V_4 - V_5 + V_6$	75	S_9, S_2, S_{11}, S_8	$V_1 + V_4 - V_2 - V_5 + V_6$
35	S_5, S_{10}, S_7, S_{12}	$-V_4 + V_5 - V_6$	76	S_5, S_{10}, S_3, S_{12}	$-V_4 + V_5 + V_2 - V_3 - V_6$
36	S_9, S_2, S_7, S_4	$V_1 + V_4 - V_2 + V_3$	77	S_9, S_2, S_{11}, S_4	$V_4 + V_1 - V_2 - V_5 + V_6 + V_3$
37	S_1, S_6, S_3, S_{12}	$-V_1 + V_2 - V_3 - V_6$	78	S_1, S_{10}, S_3, S_{12}	$-V_4 - V_1 + V_2 + V_5 - V_6 - V_3$
38	S_9, S_2, S_{11}, S_{12}	$V_1 + V_4 - V_2 - V_5$	79	S_1, S_2, S_3, S_4	0
39	S_1, S_{10}, S_3, S_4	$-V_1 - V_4 + V_2 + V_5$	80	S_5, S_6, S_7, S_8	0
40	S_9, S_2, S_7, S_{12}	$V_1 + V_4 - V_2 - V_6$	81	$S_9, S_{10}, S_{11}, S_{12}$	0
41	S_5, S_2, S_{11}, S_8	$V_1 - V_2 - V_5 + V_6$	.	.	.

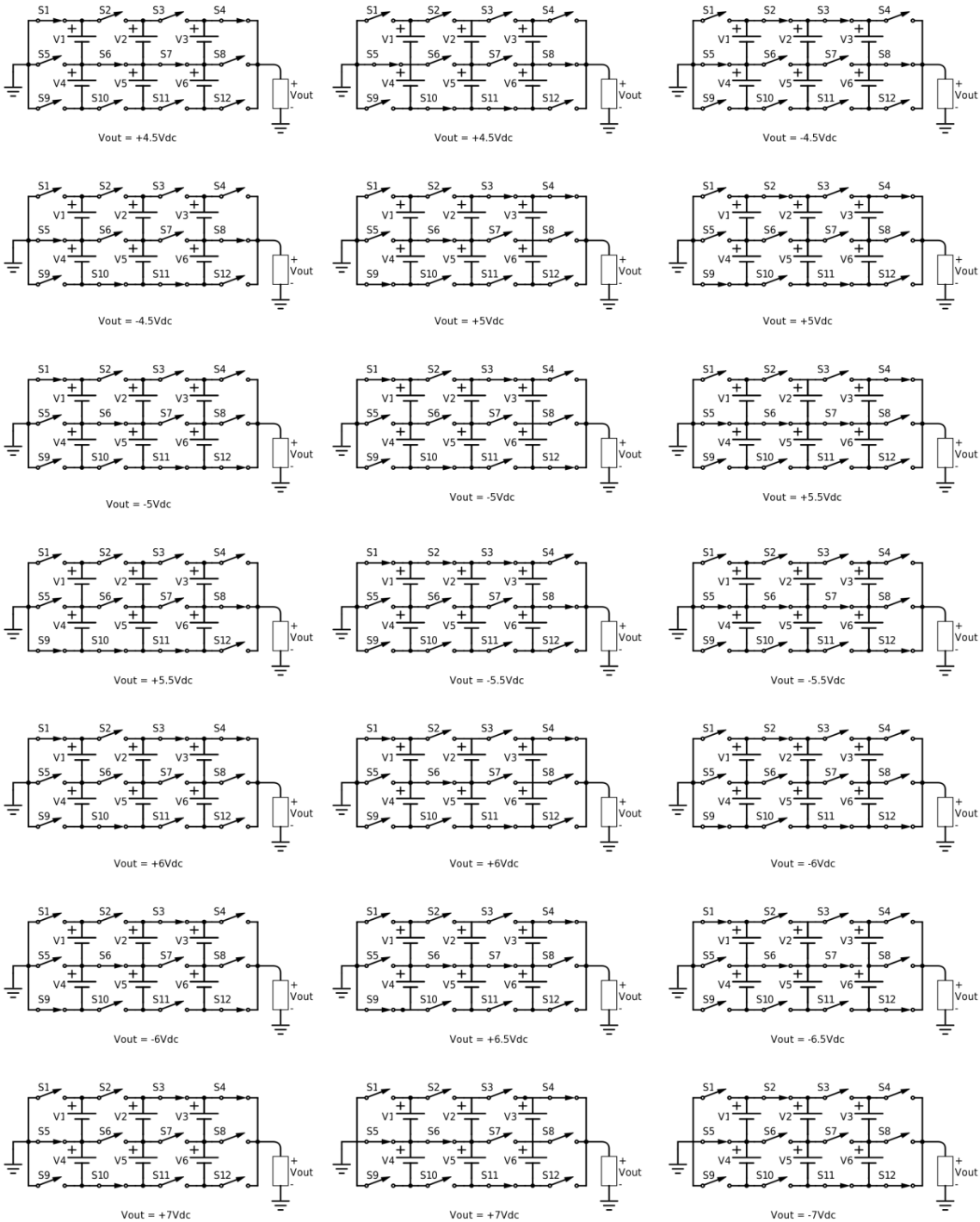


Figure 6:Various operating modes of the multilevel inverter (Fig. 4) with the corresponding output voltage and switching arrangement.

3- Results and Discussion

In this section, computer simulation of the proposed structure is presented. All simulations are performed in the MATLAB software's SIMULINK environment. In this paper, insulated gate bipolar transistor (IGBT) switches with a parallel diode for reverse current is used for switches of multilevel inverters. Some of the semiconductor switches in the presented topology necessarily require bidirectional switches that can block voltage and conduct current in both directions. To create such a bidirectional switches common emitter arrangement of two IGBTs is used for simulations. Pulse width modulation (PWM) switching method is one of the most popular modulation methods used in power inverters. In this method of modulation, to generate a switching signal, a sine signal is compared to a carrier signal. The PWM switching method is being used in the paper. Figure 7 shows the general block diagram to create the switching method in SIMULINK.

Figure 7: Block diagram to create the switching method in SIMULINK

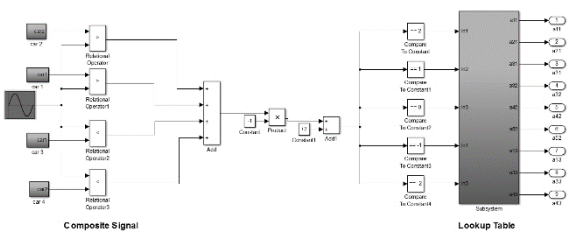
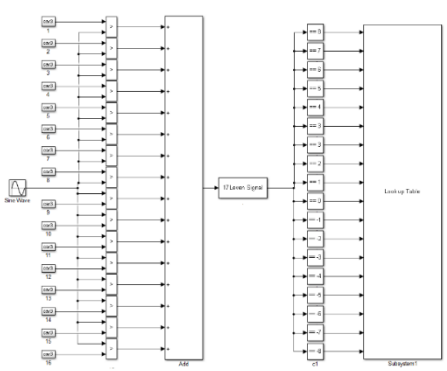
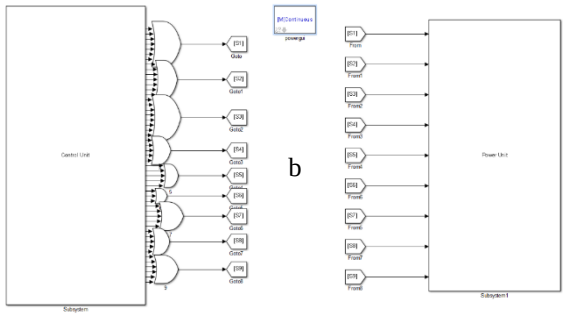


Figure 8a shows the switching implementation method using the Simulink block diagrams for the presented topology, and Figure 8b shows the general diagram of the presented topology power unit and the control unit for switching direction.

Figure 9: (a) switching implementation method using the Simulink block. (b) power unit and the control unit for switching

a





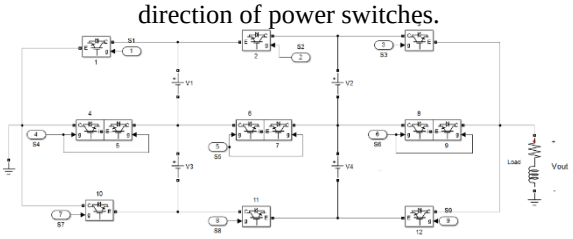
b

3-1 Results of the proposed structure 1

Figure 9 shows the topology of structure 1 with the direction of power switches. It should be noted that in order to achieve the desired voltage levels, three of the switches should be bidirectional switches capable of blocking voltage and conducting current in both directions. The source voltages are selected based on the proposed asymmetric configuration algorithm$V_1 = V_3 = 20v$ and $V_2 = V_4 = 80v$. The output is a resistive - inductive load with $R = 50\,\Omega$ and $L = 1\,mH$. The frequency of the triangular carrier is once considered as 100 Hz and once again 5000 Hz.

Figs. 10 and 11 show output voltage and current of the proposed inverter (Fig.9), respectively. Figure 10 (a) show the output voltage and its harmonic analysis for carrier frequencies of 100 Hz. THD of output voltage is 5.68%. The output voltage and its harmonic analysis for carrier frequencies of 5000 Hz are shown in Fig. 9 (b). THD of output voltage in this case is 6.99%. Fig. 11 (a) shows the output current and its harmonic analysis for carrier frequencies of 100 Hz. THD of output current is 3.72%. The output current and its harmonic analysis for carrier frequencies of 5000 Hz are shown in Fig. 11 (b). In this case, THD of output current is 1.13%. The output voltage and

Figure 8:The topology of structure 1 with the direction of power switches.



current characteristic of structure 1 is shown in table 3.

(a)
(b)

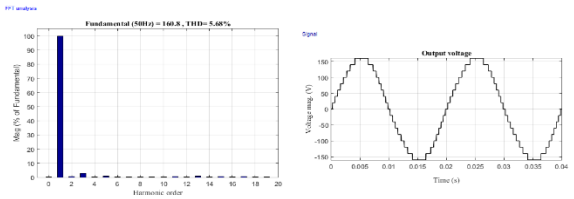
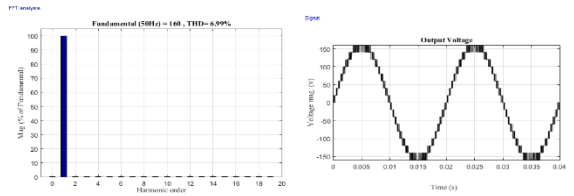


Figure 10: Output voltage and harmonic analysis of

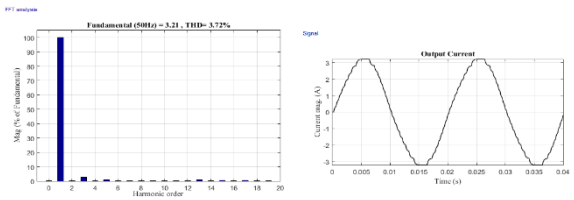


the topology of Figure 7 (a) for carrier frequency 100Hz (b) for carrier frequency 5000Hz.

Table 3: Output voltage and current characteristic of structure.

State	Carrier frequency	Characteristic of load	Peak	RMS	THD
1	100 HZ	V_{out}	160 (V)	113.7 $(V$	5.68 %
		i_{out}	3.21 (A)	2.27 (A)	3.72 %
2	5000 HZ	V_{out}	160 (V)	113.2 $(V$	6.99 %
		i_{out}	3.193 $(A$	2.258 $(A$	1.13 %

(a)



(b)

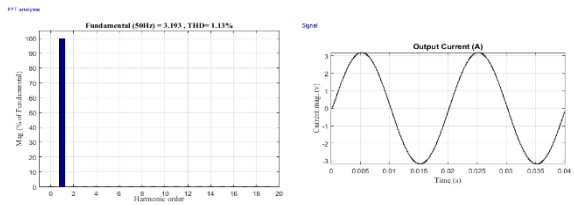


Figure 11: Output Current and harmonic analysis of the topology of Figure 7 (a) for carrier frequency 100Hz (b) for carrier frequency 5000Hz.

3-2 Results of the proposed structure 2

Figure 12 shows the topology of structure 2 with the direction of the power switches. It should be noted that four of the switches should be bidirectional switches capable of blocking voltage and conducting current in both directions in order to achieve the desired voltage levels. The source voltages are selected based on the proposed asymmetric configuration algorithm $V_1 = V_4 = 20v, V_2 = V_5 = 80v$ and $V_3 = V_6 = 110v$.
The output is a resistive - inductive load with $R = 50\,\Omega$ and $L = 1\,mH$. The frequency of the triangular carrier is once considered as 100 Hz and once again 5000 Hz.
Figs. 13 and 14 show output voltage and current of the proposed inverter (Fig.1, respectively. Figure 13 (a) show the output voltage of the inverter and its harmonic analysis for carrier frequencies of 100 Hz. THD of output voltage is 3.49% in this case. The output voltage and its harmonic analysis for carrier frequencies of 5000 Hz are shown in Fig. 12 (b). THD of output voltage in this case is 3.99%. Fig. 14 (a) show the output current and its harmonic analysis for carrier frequencies of 100 Hz. THD of output current is 2.89%. The output current and its harmonic analysis for carrier frequencies of 5000 Hz are shown in Fig. 13(b). THD of output current is 2.28%. The output voltage and current characteristic of structure 2 are shown in table 4.
In table 5 there is a comparison between the "structure 1" proposed topology and a number of multilevel

inverters reviewed in [26]. As can be seen, for a ١٧-levels output, the number of proposed topology switches has been significantly reduced.

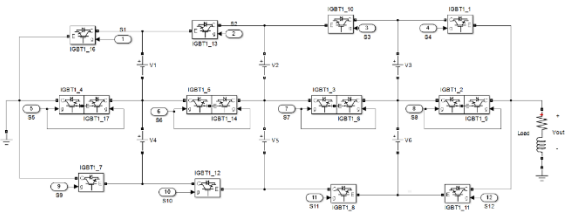
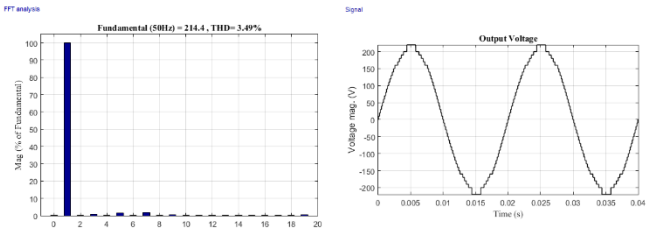
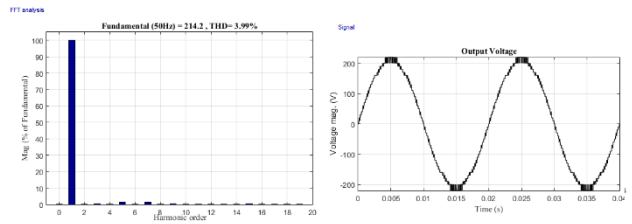


Figure 12:The topology of structure 2 with the direction of power switches.

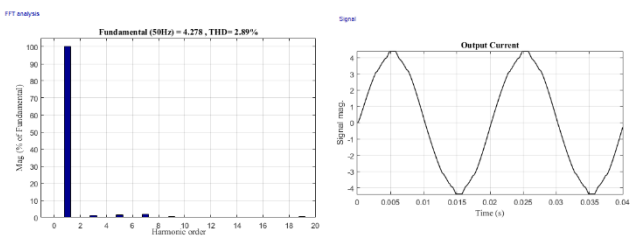


(a)

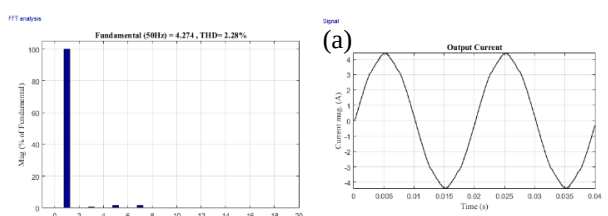


(b)

Figure 13:Output voltage and harmonic analysis of the topology of Figure 10 (a) for carrier frequency 100Hz (b) for carrier frequency 5000Hz.



(a)



(b)

Figure 14:Output current and harmonic analysis of the topology of Figure 10 (a) for carrier frequency 100Hz (b) for carrier frequency 5000Hz.

Table 4: Output voltage and current characteristic of structure 2.

State	Carrier frequency	Characteristic of load	Peak	RMS	THD
1	100 HZ	V_{out}	220 (V)	151.67 (V)	3.49 %
		i_{out}	4.28 (A)	3.025 (A)	2.89 %
2	5000 HZ	V_{out}	220 (V)	151.5 (V)	3.99 %
		i_{out}	4.28 (A)	3.022 (A)	2.28%

Table 5: Comparisons of the proposed multilevel inverters (structure) and a number of multilevel inverters reviewed in [26] (for a 17-levels output).

Number	MLI	One-directional switch	Bidirectional switch
1	MLDCL [26]	60	0
2	T-type [26]	12	48
3	SSPS [26]	75	0
4	SCSS [26]	60	0
5	CBSC [26]	0	54
6	MLM [26]	12	27
7	RV [26]	60	0
8	2SELG [26]	24	15
9	Structure 1	6	3

Table 6: Comparisons of the proposed multilevel inverters (structure) and a number of multilevel inverters reviewed in [26] (for a 43-levels output).

Number	MLI	One-directional switch	Bidirectional switch
1	MLDCL [26]	138	0
2	T-type [26]	12	126
3	SSPS [26]	192	0
4	SCSS [26]	138	0
5	CBSC [26]	0	132
6	MLM [26]	12	66
7	RV [26]	138	0

8	2SELG [26]	24	54
9	Structure 1	8	4

4- Conclusion

Because of the rise in electricity consumption and the use of DC to AC conversion, there has been a surge in interest in multilevel inverters in recent years. In this regard, this paper, present a new general topology based on the expansion of a full bridge cell. Two special cases of this general topology have been investigated. Also, to achieve the maximum output levels of these two special cases, asymmetric source configuration algorithms are provided separately for each of the structures. The structure 1, consists of nine power switches and four DC voltage sources. By using the asymmetric source configuration algorithm, a 17-level output voltage is synthesized. Three switches of structure 1 should be bidirectional switches with the capability of blocking voltage and conducting current in both directions. Structure 2, consists of twelve power switches and six DC voltage sources. By using a presented asymmetric source configuration algorithm, 41-level output with equal step and a 43-level output with two uneven levels at the beginning and the end are obtained. Structure 2's four switches should be bidirectional, capable of blocking voltage and conducting current in both directions. Two special cases of this general topology have significantly reduced the number of electronic elements of power compared to conventional structures and new structures.

5. ACKNOWLEDGEMENT

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References

[1] Baker, R.H., Bannister, L.H.: *'Electric power converter'* , US Patent 3 867 643, February 1975.

[2] Rodriguez, J., Bernet, S., Wu, B., Pontt, J.O., Kouro, S.: *'Multilevel voltage-source-converter topologies for industrial medium-voltage drives'*, *IEEE Trans. Ind. Electronics*., 2007, 54, (6), pp. 2930 –2945.

[3] Cheng, Y., Qian, C., Crow, M.L., Pekarek, S., Atcitty, S.: *'A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage'*, *IEEE Trans. Ind. Electronics*., 2006, 53, (5), pp. 1512 –1521.

[4] De, S., Banerjee, D., Siva Kumar, K., Gopakumar, K., Ramchand, R., Patel, C.: *'Multilevel inverters for low-power application'*, *IET Power Electronics*., 2011, 4, (4), pp. 384 –392.

[5] Palanivel, P., Dash, S.S.: *'Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques'*, *IET Power Electronics*., 2011, 4, (8), pp. 951 –958.

[6] Gupta, K.K., Jain, S.: *'Topology for multilevel inverters to attain maximum number of levels from given DC sources'*, *IET Power Electronics*., 2012, 5, (4), pp. 435 –446.

[7] Rabinovici, R., Baimel, D., Tomasik, J., Zuckerberger, A.: *'Thirteen-level cascaded H-bridge inverter operated by generic phase shifted pulse-width modulation'*, *IET Power Electronics*., 2013, 6, (8), pp. 1516 – 1529.

[8] Banaei, M.R., Khounjahan, H., Salary, E.: *'Single-source cascaded transformers multilevel inverter with reduced number of switches'*, *IET Power Electronics*., 2012, 5, (9), pp. 1748 –1753.

[9] Sadigh, A.K., Dargahi, V., Abarzadeh, M., Dargahi, S.: *'Reduced DC voltage source flying capacitor multicell multilevel inverter: analysis and implementation' IET Power Electronics*., 2014, 7, (2), pp. 439 –450.

[10] Al-Judi, A., Nowicki, E.: *'Cascading of diode bypassed transistor-voltage-source units in multilevel inverters'*, *IET Power Electronics*., 2013, 6, (3), pp. 554 –560.

[11] Ajami, A., Oskuee, M.R.J., Mokhberdoran, A., van den Bossche, A.*: 'Developed cascaded multilevel inverter topology to minimise the number of circuit devices*
and voltage stresses of switches', IET Power Electronics., 2014, 7, (2), pp. 459 –466.

[12] Shalchi Alishah, R., Nazarpour, D., Hosseini, S.H., Sabahi, M.: *'New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels'*, *IET Power Electron.*, 2014, 7, (1), pp. 96 –104.

[13] Gupta, K.K., Jain, S.: *'Comprehensive review of a recently proposed multilevel inverter'*, *IET Power Electronics*., 2014, 7, (3), pp. 467 –479.

[14] Odeh, C.I., Nnadi, D.B.N.: *'Single-phase 9-level hybridised cascaded multilevel inverter'*, *IET Power Electronics*., 2013, 6, (3), pp. 468 –477.

[15] Kalpesh Y. Raval; V.J. Ruvavara; *'Novel Multilevel Inverter Design with Reduced Device Count'*, 2018 International Conference on Current Trends towards Converging Technologies (ICCTCT), 1-3 March 2018

[16] Tohid Qanbari; Behrouz Tousi; *'Single-Source Three-Phase Multilevel Inverter Assembled by Three-Phase Two-Level Inverter and Two Single-Phase Cascaded H-Bridge Inverters'*, IEEE Transactions on Power Electronics, Volume: 36, Issue: 5, May 2021
[17] Gui-Jia, Su;, *'Multilevel DC-link inverter'*, Industry Applications, *IEEE Transactions* on, vol. 41, no. 3, pp. 848- 854, May-June 2005.
[18] Ounejjar, Y.; Al-Haddad, K.: *'A novel high energetic efficiency multilevel topology with reduced impact on supply network'*, in Annual Conference of *IEEE Industrial Electronics*, 2008. IECON 2008. 34th, Nov 2008.
[19] Ounejjar, Y.; Al-Haddad, K.: *'A new high power efficiency cascaded U cells multilevel converter'*, in *Industrial Electronics*, 2009. ISIE 2009. IEEE International Symposium on, July 2009.
[20] Ounejjar, Y.; Al-Haddad, K.; Gregoire, L.A.: *'Novel three phase seven level PWM converter'*, in *Electrical Power and Energy Conference (EPEC)*, 2009 IEEE, Oct 2009.
[21] Ounejjar, Y.; Al-Haddad, K.: *'Multilevel hysteresis controller of the novel seven-level packed U cells converter', International Symposium in Power Electrical Drives Automation and Motion (SPEEDAM)*, June 2010.
[22] Ounejjar, Y.; Al-Haddad, K.; Gréoire, L.A.; *'Packed U Cells Multilevel Converter Topology: Theoretical Study and Experimental Validation', IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1294-1306, April 2011.
[23] Gupta, K.K.; Jain, S.: *'Topology for multilevel inverters to attain maximum number of levels from given DC sources'*, *IET Power Electronics*, vol. 5, no. 4, pp. 435 - 446, 2012.
[24] Khosroshahi, M.: *'Crisscross cascade multilevel inverter with reduction in number of components'*," *IET Power Electronics*, vol. 7, no. 12, pp. 2914 - 2924, 2014.
[25] Gautam, S.P.; Kumar, L.; Gupta, S.: *'Hybrid topology of symmetrical multilevel inverter using less number of devices'*, *IET Power Electronics*, vol. 8, no. 11, pp. 2125 - 2135, 2015.
[26] Gupta, K. K.; Ranjan, A.; Bhatnagar, P; Sahu L. K.; Jain, S.: *'Multilevel Inverter Topologies with Reduced Device Count: A Review'*, *IEEE Transactions on Power Electronics*, Vol. 31, No. 1, Jan. 2016.