A Novel Interleaved DC-DC Converter with High Voltage Gain for Photovoltaic System Applications

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Abstract

In this paper, a high step-up DC-DC converter is proposed for use in photovoltaic systems. In the proposed converter, the interleaving technique is used to reduce the input current ripple. To increase the output voltage gain, a combination of two voltage multipliers is used in the middle part of the converter. Also, because of the low voltage stress of the switches and diodes in the proposed converter, switches with lower conduction resistance and diodes with lower voltage drop can be used to construct the proposed converter to increase the efficiency of the converter. To confirm the operation of the proposed converter, the simulation results with MATLAB software are presented in this paper. A simulated version of the proposed converter can increase the input voltage below about 20 volts to a voltage level of 400 volts. The low voltage stress on semiconductor elements, high voltage gain, and low input current ripple are the critical features of the proposed converter.

1. Introduction

Today, many power plants use fossil fuels to generate electricity. The depletion of fossil fuel sources and the adverse effects of burning these fuels on the environment has led to more attention being paid to clean and renewable energy sources such as photovoltaics. Fig 1 shows an example of the application of photovoltaic systems. Due to the low voltage level produced by photovoltaic arrays, DC-DC step-up converters increase the voltage level. Finally, the output of DC-DC step-up converters can be used to power DC loads, or by using a DC-AC converter, it can be connected to the power grid and power AC loads.
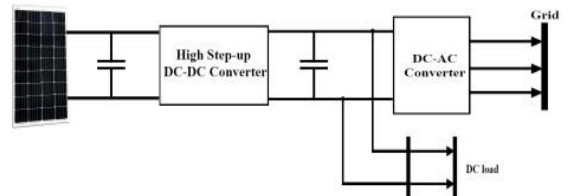

Figure 1. A typical high step-up dc-dc converter with a photovoltaic system.

Due to the importance of DC-DC converters in photovoltaic systems, there is a need for more research in this area and features such as high voltage gain should be considered. Achieving a high voltage DC-DC converter that performs better than

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other DC-DC converters used in photovoltaic systems is the most important goal of this article.

The converters proposed in the articles use various methods to increase the voltage gain. The following is an overview of these articles and the methods used in them.

Numerous converters with high voltage gain have been introduced in various articles that have used various methods to increase the voltage level in their structure. In [1-3], built-in transformers increased the voltage level. In [4-6], the switched capacitor method improves the voltage gain. Another method of increasing the voltage level is coupling inductors, which are commonly used in DC-DC converters. In [7-10], this technique has been applied to improve the output voltage gain. Voltage multipliers, which are mainly composed of diodes and capacitors, are another method of increasing the voltage level, which is widely used in high step-up DC-DC converters[11-17]. [18, 19] used a multi-stage or multi-level method to increase the voltage level. In this method, the connection of several step-up converters of the same or different is used to increase the output voltage gain. The interleaved method is one of the techniques to increase the voltage gain. In this method, n parallel phases are used in the input part of the converter, and according to the switching method used in these converters, the input current ripple is reduced, and as a result, smaller inductors can be used to increase the converter power density[3], [6], [7], [15], [17].

Due to the low output voltage level of solar panels, DC- DC step-up converters are used to increase the voltage level. Therefore, having a DC-DC converter with high voltage gain can facilitate the process of energy production in photovoltaic systems.

According to the review in the previous researches, the interleaved structure can be selected as the most suitable option for use in photovoltaic systems. Because in this structure, the input current ripple is

greatly reduced and the life of the photovoltaic panels is increased. The interleaved structure can also be combined with other methods of voltage increase. Therefore, by combining the interleaved

method with other voltage increase methods, a suitable converter with high voltage gain for use in photovoltaic systems can be achieved.

In this paper, an interleaved step-up DC-DC converter is introduced. The interleaved technique used in this converter reduces the input current ripple, and the output voltage gain of the converter is increased by using voltage multipliers. Features of this converter include high voltage gain, low input current ripple and low voltage stress on semiconductor components. The existence of these features has made the proposed converter a suitable option for use in photovoltaic systems.

The rest of sections the paper are arranged as follows. In section 2, the proposed converter and its operating principles are introduced. In Section 3, the steady-state analysis of the proposed converter is performed. In Section 4, the proposed converter is compared with some other converters of the same type. The simulation results with MATLAB software are presented in Section 5, and Finally, a general conclusion is presented in Section 6.

2. The Proposed Converter and Its Operating Analysis

The schematic of the proposed converter is shown in Fig 2. This converter consists of two switches, five diodes, six capacitors, and three inductors. In the input part of the proposed converter, the interleaving technique reduces the input current ripple, and in the output part, voltage multipliers are used to increase the voltage gain. The signals applied to the gates of the switches are interleaved with 180 degrees phase shift.

The proposed converter has four operating modes, and the time intervals T1, T2, T3, and T4 are the times of each of these modes. Based on interleaved method, time interval T1 is equal to time interval T3 and time interval T2 is equal to time interval T4. The key waveforms of the proposed converter and the equivalent circuit corresponding to each of the operating modes are shown in Figs. 3 and 4, respectively. According to the above, the duty cycle range of the proposed converter is determined as follows:

$$T_1 = T_3 = d_1 T = d_3 T \tag{1}$$

$$d_1 = d_3 = d_{13} \tag{2}$$

$$T_2 = T_4 = d_2 T = d_4 T = (1-D)T \tag{3}$$

$$d_2 = d_4 = 1 - D \tag{4}$$

$$DT = d_1 T + d_2 T + d_3 T = 2d_{13}T + d_2 T \tag{5}$$

$$D = 0.5 + d_{13} \tag{6}$$

Where d1, d2, d3, and d4 are the duty cycles for each time interval. Equation (6) shows that the value of D is limited between 0.5 and 1. The operating modes of the proposed converter are described as following:

Mode 1[$t_0 - t_1$]: During this mode, S1, and S2 are turned on and the input inductors L1 and L2 are charged, and all diodes are in reverse bias and do not conduct.

In this operating mode, the output load is supplied by output capacitor C6. This mode ends when S2 is turned off, and D2 and D4 start conducting at t=t1. According to Fig. 4(a), the equations of this operating mode are extracted as follow:

$$V_{L1} = V_{L2} = V_{in} \tag{7}$$

$$V_{L3} = V_{C1} - V_{C2} - V_{C3} \tag{8}$$

$$V_o = V_{C6} \tag{9}$$

Mode 2[$t_1 - t_2$]: In this operating mode, S1, D2 and D4, are on, and S2, and other diodes are off. In this case, inductor L1 is still charged by the input source, but inductor L2 starts discharging when switch S2 is turned off. Because output diode D5 is off in this operating state, output capacitor C6 continues to supply the output load of the converter and is discharged. This state ends at the moment of t2 when S2 is turned on and D2, and D4 are turned off. According to Fig 4(b), the equations related to this operating mode are extracted as follows:

$$V_{L1} = V_{in} \tag{10}$$

$$V_{L2} = V_{in} + V_{C2} - V_{C1} \tag{11}$$

$$V_{L3} = -V_{C3} \tag{12}$$

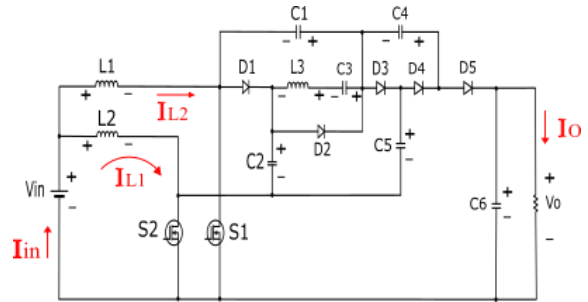$$V_{C5} = V_{C2} + V_{C4} \tag{13}$$

$$V_o = V_{C6} \tag{14}$$

Figure 2. The proposed converter.

Mode 3[$t_2 - t_3$]: This operating mode is the same as the first operating mode, and the relationships extracted for the first operating mode are also valid for this mode. This mode ends at the moment of t3, when switch S1 is turned off and D1, D3, and D5, are turned on. The equivalent circuit for this operating mode is shown in Fig 4(c).

Mode 4[$t_3 - t_4$]: In this mode, S2, D1, D3, and D5 are on, and S1 and other diodes are off. In this case, the inductor L1 is discharged when the switch S1 is turned off, and the energy stored in it is transferred to the secondary section of the circuit, and because the output diode is on in this mode, the output capacitor C6 is charged. According to Fig 4(d), the equations related to this operating mode are extracted as follows:

$$V_{L1} = V_{in} - V_{C2} = V_{in} + V_{C1} + V_{C4} - V_o \tag{15}$$

$$V_{L2} = V_{in} \tag{16}$$

$$V_{L3} = V_{C1} - V_{C3} = V_{C5} - V_{C3} - V_{C2} \tag{17}$$

$$V_{C5} = V_{C1} + V_{C2} \tag{18}$$

$$V_o = V_{C6} = V_{C4} + V_{C5} \tag{19}$$

3. Steady-State Analysis of The Proposed Converter

3.1. Voltage Gain Analysis

Considering that the average voltage of an inductor in a switching period is equal to zero and using the relationships obtained for each of the operating modes in the previous section, the voltage values of

the capacitors and the voltage gain of the converter are calculated in this section.

The time interval related to each of the operating modes is considered as follows:

$$[t_0, t_1] = [t_2, t_3] = \frac{2D-1}{2}T \quad (20)$$

$$[t_1, t_2] = [t_3, t_4] = (1-D)T \quad (21)$$

By applying the volt-second law to the inductors L1, L2, and L3, the following equations are obtained:

$$\langle V_{L1} \rangle_T = 0 \rightarrow V_{C2} = \frac{V_{in}}{1-D} \quad (22)$$

$$\langle V_{L2} \rangle_T = 0 \rightarrow V_{C1} = \frac{2V_{in}}{1-D} \quad (23)$$

$$\langle V_{L3} \rangle_T = 0 \rightarrow V_{C3} = \frac{V_{in}}{1-D} \quad (24)$$

By placing (22) and (23) in (18), the value of V_{C5} is obtained as follows:

$$V_{C5} = V_{C1} + V_{C2} = \frac{3V_{in}}{1-D} \quad (25)$$

By placing (22) and (25) in (13), the value of V_{C4} is obtained as follows:

$$V_{C4} = V_{C5} - V_{C2} = \frac{2V_{in}}{1-D} \quad (26)$$

By placing (25) and (26) in (19), the value of V_{C6} and the voltage gain of the proposed converter are obtained as follows:

$$V_O = V_{C6} = V_{C4} + V_{C5} = \frac{5V_{in}}{1-D} \quad (27)$$

$$M = \frac{V_O}{V_{in}} = \frac{5}{1-D} \quad (28)$$

The gain change curve versus the duty cycle of the converter is shown in Fig 5. The proposed converter

has a high step-up voltage gain without using coupled inductors and transformers.

3.2. *Voltage Stress Analysis of the Semiconductors*

The voltage stress of the proposed converter switches and diodes is calculated as follows:

$$V_{D_{s1}} = V_{C2} = \frac{V_{in}}{1-D} = \frac{V_O}{5} \quad (29)$$

$$V_{D_{s2}} = V_{C1} - V_{C2} = \frac{V_{in}}{1-D} = \frac{V_O}{5} \quad (30)$$

$$V_{D1} = V_{D2} = V_{D3} = V_{D4} = \frac{2V_{in}}{1-D} = \frac{2V_O}{5} \quad (31)$$

$$V_{D5} = \frac{V_{in}}{1-D} = \frac{V_O}{5} \quad (32)$$

As can be seen, the stresses on the semiconductors are low, which may yield a higher overall converter efficiency.

3.3. *Boundary Conduction Mode Analysis*

In the analyzes performed in the previous section, the converter is considered in continuous conduction mode. In this section, the critical value of the input inductors of the proposed converter for operation in continuous conduction mode is determined. The amount of input inductors is calculated as follows:

$$\frac{1}{2}\Delta i_{L,Crit} = \frac{I_{in}}{2} \quad (33)$$

$$\frac{DV_{in}}{L_{Crit}f_S} = \frac{5}{1-D}I_{out} \quad (34)$$

Using (32) in (34), the critical inductance is obtained as follows:

$$L_{Crit} = \frac{D(1-D)^2}{25f_S}R_{out} \quad (35)$$

4. Performance Comparison

In this section, the results of comparing the proposed converter with five other converters are presented. Table 1 compares the converters in terms of voltage gain, the number of elements used, and voltage stress of semiconductor components.
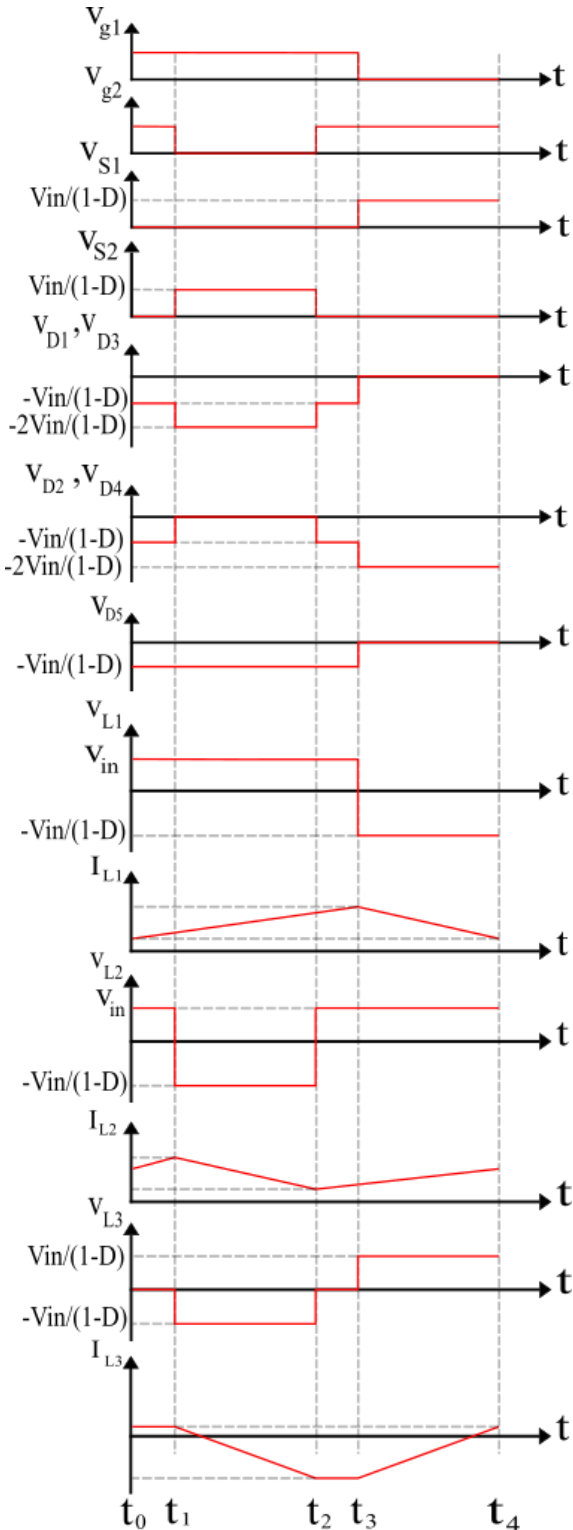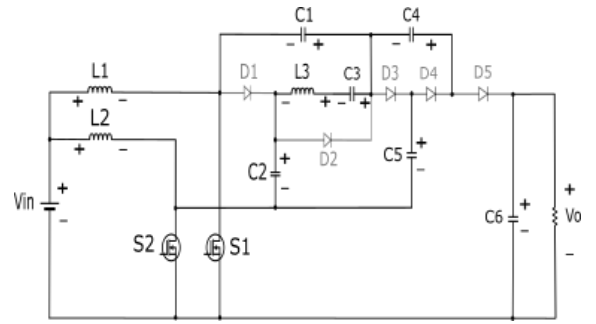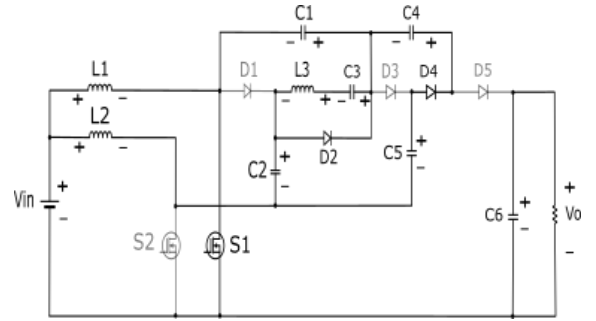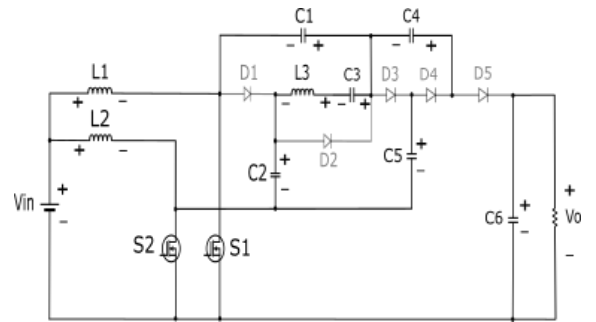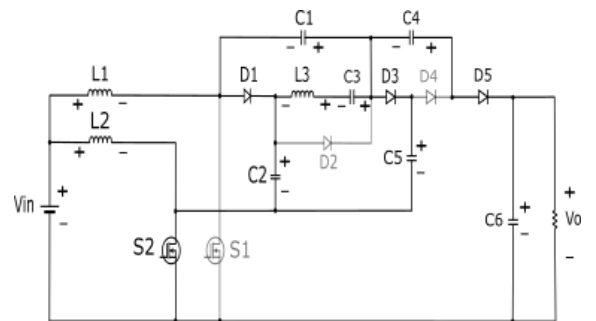
Figure 3. The key waveforms of the proposed converter.

Figure 4. The equivalent circuits of the proposed converter in different operating modes: (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4.
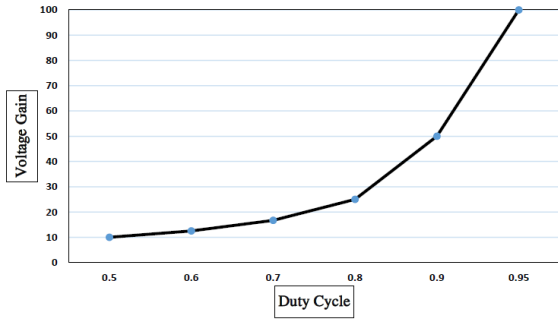
Figure 5. The voltage gain of the proposed converter.

It should be noted that in comparing the voltage stress of switches and diodes in the proposed converter with the other compared converters, the switch and diode with the highest voltage stress are selected from each converter. According to the results presented in Table 1, the switches used in the proposed converter have the lowest voltage stress among the compared converters. To better compare the converters, the conversion gain diagram of the converters is shown in Fig 6. According to this figure, it is clear that the proposed converter has a higher voltage gain than other converters.

5. Design Consideration
5.1. Design of Input Inductors
The current waveform passing through inductors L1 and L2 and the total input current of the converter are shown in Fig 7. Values I_{max} and I_{min}, which are

The inductor current i_{L1} in the first, second, and third operating modes is determined as (36):

$$i_{L1}(t) = \frac{I_{max} - I_{min}}{DT} t + I_{min} \tag{36}$$

The inductor current i_{L2} in the second operating mode is determined as (37):

$$i_{L2}(t) = \frac{I_{min} - I_{max}}{(1-D)T}(t - \frac{T}{2}) + I_{min} \tag{37}$$

Equal to the maximum current and minimum current passing through the inductors, respectively, are defined according to Fig 7.

To calculate the input current ripple and the values of input inductors of the proposed converter, the second operating mode is considered. According to (38), the input current of the converter is equal to the sum of the currents passing through each of the input inductors.:

$$i_{in} = i_{L1} + i_{L2} \tag{38}$$

The value of the inductors currents at the beginning of the second operating mode $(t = \frac{2D-1}{2}T)$, are equal to:

$$i_{L1}(t = \frac{2D-1}{2}T) = \frac{(I_{max} - I_{min})(2D-1)}{2D} + I_{min} \tag{39}$$

$$i_{L2}(t = \frac{2D-1}{2}T) = I_{max} \tag{40}$$

And the value of the total input current of the converter at the beginning of the second operating mode is obtained as (41):

$$i_{in}(t = \frac{2D-1}{2}T) = I_{in_{max}} = \frac{I_{min} - I_{max}}{2D} + 2I_{max} \tag{41}$$

The value of the inductors current at the end of the second operating mode $(t = \frac{T}{2})$, is equal to:

$$i_{L1}(t = \frac{T}{2}) = \frac{I_{max} - I_{min}}{2D} + I_{min} \tag{42}$$

$$i_{L2}(t = \frac{T}{2}) = I_{min} \tag{43}$$

And the value of the total input current of the converter at the end of the second operating mode is obtained as (44):

$$i_{in}(t = \frac{T}{2}) = I_{in_{min}} = \frac{I_{max} - I_{min}}{2D} + 2I_{min} \tag{44}$$

Using (41) and (44), the input current ripple of the proposed converter is calculated as follows:

Table 1. Converter performance comparison.

| Topology	Proposed converter	[3]	[6]	[7]	[15]	[17]
Total number of components	16	14	34	20	14	23
Switches	2	2	6	4	3	2
Diodes	5	4	14	7	4	8
Capacitors	6	3	8	2	4	9
Inductors	3	2	6	1	3	4
Coupled inductors or built-in transformers	0	3	0	6	0	0
Number of magnetic cores	3	3	6	4	3	4
Voltage gain	$\dfrac{5}{1-D}$	$\dfrac{2+n}{1-D}$	$\dfrac{3+D}{1-D}$	$\dfrac{1+Dn}{1-D}$	$\dfrac{4}{1-D}$	$\dfrac{1+3D}{1-D}$
Voltage stress of switches	$\dfrac{V_O}{5}$	$\dfrac{V_o}{2+n}$	$\dfrac{V_o}{3+D}$	$\dfrac{V_o}{1+nD}$	$\dfrac{V_o}{4}$	$\dfrac{V_o}{1+3D}$
Maximum Voltage stress across diodes	$\dfrac{2V_O}{5}$	V_o	$\dfrac{2V_o}{3+D}$	$\dfrac{2(1+nD)V_o}{1-nD}$	$\dfrac{V_o}{2}$	$\dfrac{DV_o}{1+3D}$
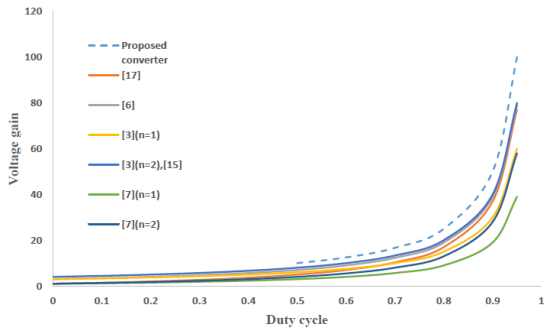
Figure 6. Comparison of the voltage gain of different topologies and proposed topology for various duty cycles.

$$Di_{in} = I_{in_{max}} - I_{in_{min}} = \frac{(2D-1)(I_{max}-I_{min})}{D} \qquad (45)$$

And the inductors current ripple is calculated as follows:

$$i_{L2}(t=t_2) = I_{min} = \frac{1}{L_2}(\int_{t_1}^{t_2} \frac{-DV_{in}}{1-D} dt) + I_{max} \qquad (46)$$

$$\Delta i_L = I_{max} - I_{min} = \frac{DTV_{in}}{L_2} \qquad (47)$$

By placing (47) in (45) and assuming(L1=L2=L) and $(T=\dfrac{1}{f_s})$, the input current ripple and the value of the input inductors, are calculated as follows:

$$\Delta i_{in} = \frac{(2D-1)V_{in}}{Lf_s} \qquad (48)$$

$$L_1 = L_2 = L = \frac{(2D-1)V_{in}}{f_S \Delta V_{in}} \qquad (49)$$
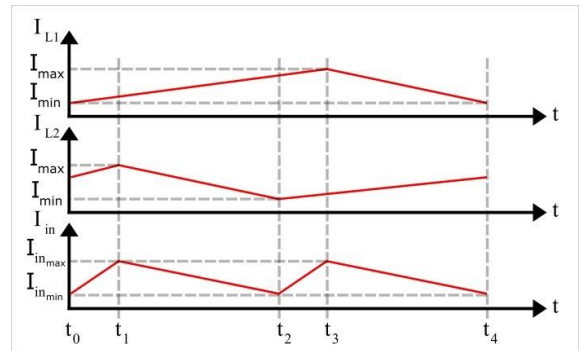

Figure 7. The current waveform passing through inductors L1, and L2, and the converter input current waveform.

5.2. Design of Output Capacitor

In the proposed converter, diode D5 is turned on only in the fourth operating mode, and capacitor C6 is charged. In other operating modes, capacitor C6 supplies the output load and starts to discharge. Therefore, to calculate the output voltage ripple and the output capacitor value, the first, second, and third operating modes are considered. At the beginning of the first operating mode, the output capacitor voltage has its maximum value, at the end of the third operating mode, the output capacitor voltage has its minimum value. The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_C(t) = \frac{1}{C} \left(\int_{t0}^{t1} i_c(t)dt + \int_{t1}^{t2} i_c(t)dt + \int_{t2}^{t3} i_c(t)dt \right) \qquad (50)$$

The output capacitor current in these three operating modes is equal to:

$$i_{C6} = -I_O \qquad (51)$$

Where I_O is the output current. Using the above relations, output voltage ripple and the output capacitor value is determined as follows:

$$\Delta V_O = \frac{DI_O}{fC_O} \qquad (52)$$

$$C_O = C_6 = \frac{DI_O}{f\Delta V_O} \qquad (53)$$

Table 2. Specification of the simulation model.

Components	Parameters
Power	396.6 W
Input-output voltage	20 V
Switching frequency	24 kHz
Duty cycle	75%
Capacitors	$C_1 = C_2 = C_3 = C_4 = C_5 = 150\mu F$ $C_6 = 220\mu F$
Inductors	$L_1 = L_2 = L = 100\mu H$
Power MOSFETs	$R_{DS(ON)} = 0.011\Omega$
Power diodes	$V_F = 0.8V$

6. Simulation Results

To prove the performance of the proposed converter, the converter is simulated using MATLAB software. The various parameters required for simulation are presented in Table 2.

The simulations results confirm the performance of the proposed converter. The output voltage waveform is shown in Fig 8(a). The output voltage is equal to 396.4V. The total input current is shown in Figure 8 (b), which is equal to 21.47A. The

inductors L1, L2, and L3 voltage waveforms are shown in Fig 8(c-e), respectively.
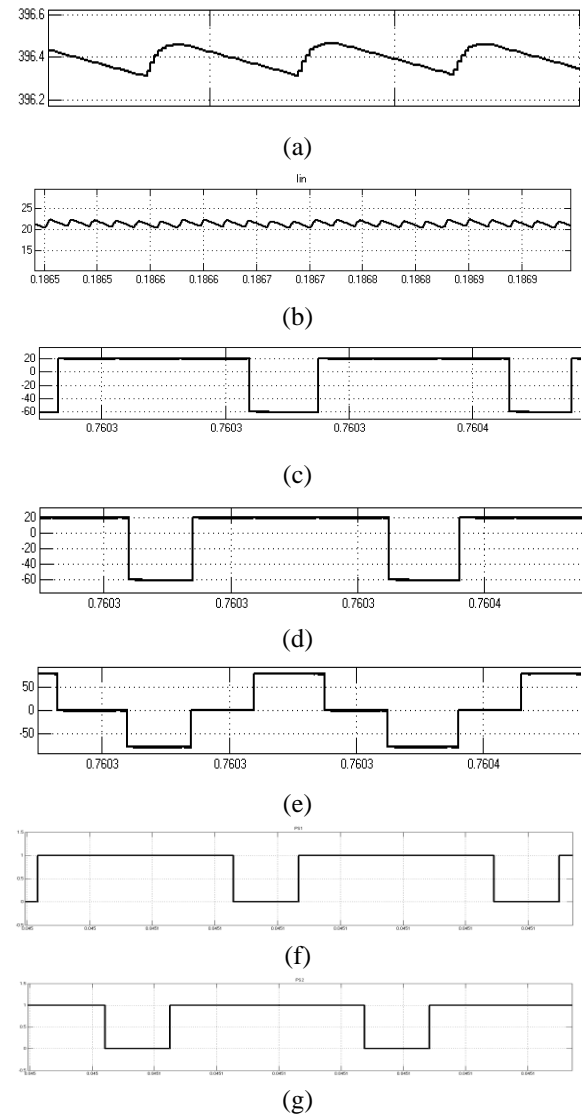
(a)

(b)

(c)

(d)

(e)

(f)

(g)

Figure 8. Simulation results of: (a) V_{out} , (b) I_{in} , (c) V_{L1} , (d) V_{L2} , (e) V_{L3} , (f) Pulse on switch S_1 , (g) Pulse on switch S_2 .
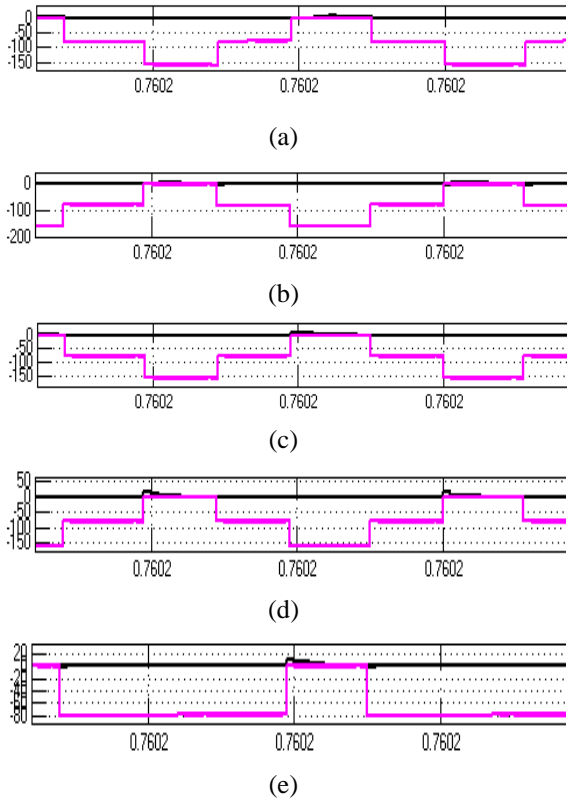
(a)

(b)

(c)

(d)

(e)

Figure 9. The voltage waveform of the diodes: (a) V_{D1}, (b) V_{D2}, (c) V_{D3}, (d) V_{D4}, (e) V_{D5}

Fig 8(f-g) show switches pulses and it can be seen that duty cycle is equal to 75%. The voltage of diodes D1, D2, D3, D4, and D5 waveform is shown in Fig 9. The voltage stresses on diodes D1, D2, D3 and D4 are equal to $2V_o/5$ and it is $V_o/5$ for D5. The voltage of the switches S1 and S2 is shown in Fig 10. According to these figures, the voltage stress on the switches is 80V. It is apparent that the voltage stress on semiconductors of the proposed converter is lower than other structures compared in this paper. A comparison between theoretical and simulation results is presented in Table 3. Comparing the simulation results with theoretical analyzes confirms the analyzes performed in the previous sections.

Fig 11 shows the curves of the efficiency of the proposed converter versus output load, the full load efficiency of the proposed converter is equal to 91.46%.

Table 3. Comparison of simulation results with mathematical analysis.

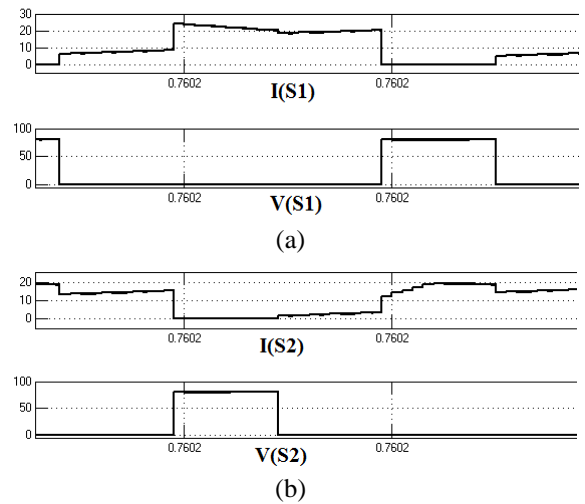| Parameter	Mathematical Analysis	Simulation Results
V_O	400V	396.4V
I_{in}	20A	21.47A
V_{DS1}, V_{DS2}	80V	80V
$V_{D1}, V_{D2}, V_{D3}, V_{D4}$	160V	≈160V
V_{D5}	80V	≈80V
V_{C1}, V_{C4}	160V	≈158.5V
V_{C2}, V_{C3}	80V	≈79.4V
V_{C5}	240V	238V
V_{C6}	400V	396.4V

(a)

(b)

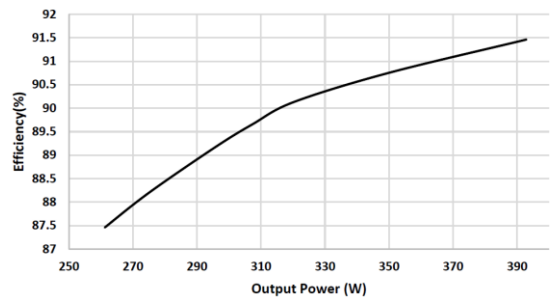Figure 10. The voltage and current waveform of the switches: (a) S1, (b) S2.

Figure 11. The efficiency of the proposed converter.

Table 3. Comparison of simulation results with mathematical analysis.

Parameter	Mathematical Analysis	Simulation Results
V_O	400V	396.4V
I_{in}	20A	21.47A
V_{DS1}, V_{DS2}	80V	80V
$V_{D1}, V_{D2}, V_{D3}, V_{D4}$	160V	$\approx$160V
V_{D5}	80V	$\approx$80V
V_{C1}, V_{C4}	160V	$\approx$158.5V
V_{C2}, V_{C3}	80V	$\approx$79.4V
V_{C5}	240V	238V
V_{C6}	400V	396.4V

7. Conclusion

In this paper, a non-isolated interleaved boost DC/DC converter is presented with reduced voltage stress on semiconductors. Due to the low voltage stresses on semiconductor components, the power circuit components can be selected to be low voltage rated; consequently, the related costs and losses would be reduced. The proposed converter was compared with several other converters in terms of the number of elements, voltage stresses on semiconductor components, and voltage gain, which showed the superiority of the proposed converter. The simulation model of the proposed converter is simulated in 400W with a 24kHz switching frequency. The simulation results were compared with the results of theoretical analysis.

Due to the low output voltage level of solar panels, DC-DC step-up converters are used to increase the voltage level. Therefore, having a DC-DC converter with high voltage gain can facilitate the process of energy production in photovoltaic systems. The proposed converter in this paper has high voltage gain, low voltage stress on semiconductor elements and low input current ripple. The existence of these features has made the proposed converter a suitable option for use in photovoltaic systems.

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