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Improved Low Voltage Ride-through Capability of PV Connected to the Unbalanced Main Grid

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Abstract

Because of the commitment between the large-scale photovoltaic power plants and the main grid to cope with different low voltage conditions in the grid, Low Voltage Ride Through (LVRT) capability of such plants is necessary. Handling this situation is more challenging when the main grid is under unbalanced conditions. In this paper, a new LVRT approach is proposed to reduce oscillations in this situation. To this end, the simultaneous positive, negative, and zero sequences control (PNZSC) method is proposed to provide a suitable reference current for eliminating oscillations of the active power, and similarly to reduce voltage oscillations of the DC side. The zero sequence control is achieved through proper inverter switching.

Also, this method limits the inverter output current to the maximum rated value. A Dual Second Order Generalized Integrator - Frequency Locked Loop (DSOGI-FLL) is used for better synchronizing of the inverter to the grid, in asymmetric faults. Besides, an interleaved DC-DC converter and a Neutral Point Clamped (NPC) Inverter are used to reduce Total Harmonic Distortion (THD) and losses. The performance of the proposed approach is confirmed using simulation of different possible scenarios in MATLAB/Simulink environment.

Keywords: LVRT, Zero Sequence Current, DSOGI-FLL, PNZSC strategy, Braking Resistor

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1. Introduction

The increasing demand for electricity and the environmental problems therefrom have increased investment in renewable energies in the last few decades. As one of the most accessible renewable energy sources, solar energy has been highly appreciated [1, 2]. The expansion of production by solar power stations has led to an increase in the level of fault current on the one hand, and an increase in the limit of switchgear and infrastructure on the other hand [3, 4]. Solar power plants connect to the AC grids in single or two stages. In the single-stage approach, the PV power plant is connected to the grid through a DC/AC converter (inverter), directly. A DC/DC converter (chopper) is installed between the solar power plant and the inverter in the

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two-stage approach to increase the DC voltage level. In [5], a review of non-isolated DC-DC converters of voltage enhancers for photovoltaic systems has been presented in which the topologies of boost, hybrid boost, three-level boost, multi-level boost, and three-level hybrid converters have been discussed. In general, in the single-stage method, oscillations in the AC grid do not influence the solar power plant performance. In case of a fault in the AC grid, the PV operating point changes subject to the new current and voltage [6]. In two-stage systems, with the presence of the chopper and its end capacitor, it is not possible to change the operating point [7]. If a transient fault occurs in the AC side, the power electronic interfaces (PEI) in the solar power stations turn off automatically, which is unacceptable given that in some areas, solar power stations are the only sources of electricity. In this regard, many countries try to prevent the automatic disconnection of solar power stations due to transient faults by providing standards in the form of grid codes. In this context, every country defines its standards subject to its power grid conditions [8]. One of the strictest standards is the Germane E.on that prevails in this industry worldwide [9]. This standard is used in this study to address LVRT capability. In two-stage systems, one of the essential issues is the AC voltage drop because of the resultant too much grid current. One of the methods for preventing voltage drop during fault occurrence is the injection of reactive power into the grid [10, 11]. Upon a fault occurrence, in addition to preventing the voltage drop, the oscillations must also be reduced. To transfer the DC power produced in a solar power plant having power electronic interfaces (PEIs) are of the essence, including 1) the booster grid DC output voltage chopper of the PV and 2) the inverter between the PV and the AC grid. Another essential part of the PV connected to the grid is the capacitors between the DC part and the inverter. The available oscillations in current and active power on the AC grid damage the semiconductor components and reduce the capacitors' durability [12, 13]. Consequently, it is essential to adopt strategies that reduce system oscillations as much as possible. The sources of the strategies must be identified to reduce system oscillations, for which separation of the current waveform sequences is a must. A method for this separation in a PV connected to a three-phase AC grid has been proposed in [14], where, first, the current values are converted into a synchronous reference frame (SRF), and next, the positive, negative, and zero sequences are separated. Setting the negative sequences sequence reference values to zero eliminates the oscillation. In that article, no reference was made to controlling the zero-sequence and reducing the oscillations. The method presented in [15] was applied to control the three-phase grid connected to the solar power plant in [14]. In this article, it is attempted to prevent the active power from exceeding the nominal value. However, a traditional inverter and chopper have been used, which cannot eliminate the oscillations. No method has been presented to control the zero-sequence flow. After separating the current sequences, the active and reactive powers are injected into the grid according to the voltage imbalance coefficient and the coefficients in proportion with the positive and negative sequence currents [13]. In this method, the objective is the reduction of the oscillations concerning the positive and negative sequence coefficients without assessing the effect of zero sequences, and the employed switching converters are traditional as well. In [16], a current-generation control strategy has been proposed to support the voltage. In this article, the positive sequence voltage of the grid increases and decreases the negative sequence. All the activities here are subjected to grid impedance, results in a reduction in the voltage unbalance force (VUF) coefficient. However, the proposed strategy needs grid impedance calculation. The proposed current control strategy limits the peak currents improving the fault passage conditions by injecting the positive and negative active and reactive components [17, 18]. Thus, no exceeding the nominal current in a grid results in preventing the PV inverter from turning OFF at current increase. Because of the flexibility and ability to balance the positive and negative components of active and reactive powers simultaneously and limit currents equally in the feasible sense, adopting this strategy is considered rational. The maximum allowable injectable current by the inverter is of no

concern. Another strategy to reduce oscillations in grid-connected solar systems is to apply a suitable PEI. The NPC inverter is connected to a Wye-Grounded transformer, and there is the possibility of zero sequence current therein. The oscillation caused by the zero-sequence current leads to oscillation in the inverter output [19, 20]. These oscillations reduce the system's DC side capacitors' durability. Upon fault occurrence, in addition to the sudden decrease in voltage that occurs in the grid side, the voltage in the DC side also increases suddenly [17]. In [18], a linearization control strategy with vital feedback has been proposed, using slip mode control and counteracts the uncertainty when passing through low voltage in PV systems connected to the grid. The proposed strategy keeps the DC voltage constant by controlling the active and reactive powers during the voltage drop. A combined control strategy, including the current model prediction control algorithm and NOT by Maximum Power Point Tracking (MPPT) algorithm, has been proposed in [21]. In [22], to prevent overvoltage in the dc section, the PV array is in the NOTMPPT position, and the appropriate output value for PV is determined by setting the proper duty cycle. In [23], a braking chopper on the dc side is also used for the sudden voltage surge in the single-stage PV system.

The proposed low voltage ride-through (LVRT) control approach is aimed at a multi-objective fault ride-through capability. The first objective is to prevent PV disconnection from the main grid due to voltage drops at faults. According to the E.ON standard, a portion of the injectable active power into the grid is allocated to reactive power. Such a strategy, together with increasing grid voltage during a fault, limits the inverter output current to the maximum rated value. The next objective is to reduce the oscillations of the injected active power, which necessitate eliminating features causing oscillations, together with promoting the non-contributive factors in this context. The negative sequence is eliminated, and the zero sequence is also countered in the inverter switches. The zero-sequence control in this regrad has been less addressed in the literature. It is evident that the zero-sequence control, next to reducing the oscillations in the three-phase AC grid connected to the PV, also reduces the oscillations in the DC part of the system. In [24], a high step-up DC-DC converter has been proposed for photovoltaic systems, by which the input current ripple is reduced using the interleaving technique.

In this study, a three-level NPC inverter and an Interleaved Boost DC/DC converter are used. These devices are of significant impact, where reducing the THD of the system is of concern. The objectives of this study are:

1- Improving LVRT capability by injection of reactive power in case of unbalanced grid conditions.

2- Reducing oscillations caused by system imbalance due to phase impedance inequality and asymmetric faults on the AC grid side using a suitable PEI, including an Interleaved Boost DC/DC converter and a three-level NPC inverter, in which the inverter output current is limited to the maximum rated value.

3- Reducing oscillations caused by the zero-sequence current flowing between NPC inverter and Wye-Grounded transformer by simultaneously controlling the three positive, negative and zero sequences, that has been done for the first time.

4- Controlling the DC side voltage oscillations and preventing a sudden increase in DC side voltage by inserting a parallel resistor in the DC side.

The rest of the article is structured as follows: the analysis of the subject system is presented in Section 2; the LVRT control strategy is proposed in Section 3 and the corresponding simulation results are presented.

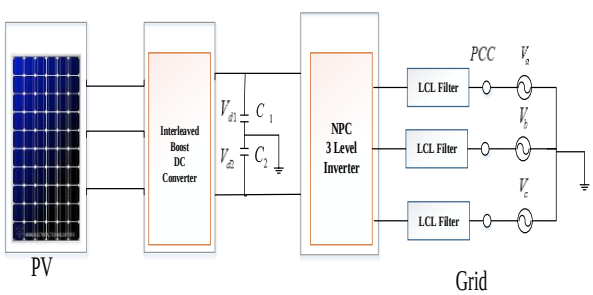


Figure 1. Two-stage PV system connected to a three-phase grid

2. Analysis of the understudied system

As observed in Figure 1, a two-stage PV system is connected to a three-phase grid. The PEI consists of a Boost Interleave converter and a three-level NPC inverter connected through a DC link capacitor.

2-1. Interleaved Boost DC / DC converter

In most cases, output voltage of photovoltaic (PV) systems is low and considering the intermittent nature of such plants boosting the voltage and MPPT are necessary [7]. In order to have a better MPPT, it is necessary to minimize switching losses as much as possible. The gain of a conventional amplifier converter is limited. High voltage output is controllable through a high duty cycle, making the switches remain ON for an extended period. If the current of the boost converter is high, the diode is faced with the reverse recovery phenomenon in this situation. This is why relying merely on the high-duty cycle is not rational [25]. The converter must generate high voltage amplitude with low ripple [26]. The switching frequency must be high to reduce the size of the inactive components. By applying the interleaved technique, the output power quality can be increased [27]. These advantages make the proposed converter a proper candidate to be applied in a PV system [28]. Interleaved amplifying converter contains many converters in parallel connection, through which the current is divided between them; thus, losses are minimized and tensions are reduced. The current ripple is reduced on the output side, reflected in the input current. The ratio of input power to the output of the interleave converter compared to the conventional converter in the same conditions and as a result the overall efficiency also increases for the above reasons. The interleaving technique is a different switching connection that improves the effective pulse frequency synchronization. By applying the interleaving technique, a percentage of the total power is managed through each switching component, according to the parallel paths' count; thus, the maximum stress and the ripple decrease, while efficiency increases. One of the primary features of applying this technique is its ability to reduce the semiconductor switches ON time and losses, and also to increase the switching durability. The relation between the output and input voltages of the converter is as follows [7]:

$$V_O = V_{in} / (1-\delta) \quad (1)$$

where V_O , V_{in} and δ are the output voltage, input voltage, and DC/DC converter duty cycle, respectively. According to Eq. (1), to increase the output voltage, the semiconductor switch ON time must be increased. The greater the switch count, the less time for each to remain ON; consequently, a three-level Interleave boost converter is applied in this study. This converter is used to increase the PV output voltage and decrease the losses and oscillations in the DC side, as shown in Figure 2.

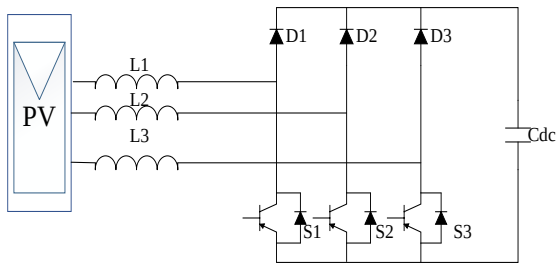


Figure 2. Boost Interleaved three-level converter

2-2. AC / AC three-level inverter converter

In recent years, multi-level inverters have become more considered due to their ability to generate waveforms with lower harmonic spectra and having access to higher levels of voltage. As a solution for increasing a converter's operating voltage, the voltage of these inverters is higher than that of the classical semiconductors' tolerable limit. This inverter consists of a set of series switches for power conversion. Increasing the step voltage by DC capacitors creates several voltage levels [27, 28]. Multi-level inverter output improves voltage quality and reduces voltage oscillations in power electronic devices. There is an inverse relationship between voltage levels and the harmonic level of the output voltage wave. Multi-level inverters have low THD at higher output voltage, efficiency, and power factor. Due to their low switching frequency, multi-level inverters are of high efficiency. As voltage levels increase, the voltage waveform has more free switching angles. This converter is used to remove

harmonics as much as possible.

3. The LVRT Control strategy (PNZSC)

The E.ON standard is adopted for LVRT and reactive power injection in PNZSC strategy. Because of inequality in the grid's phases impedance connected to the solar power plant, a unique situation is encountered that causes oscillations in the grid current connected to PV due to the negative and zero sequences current. The negative sequence is eliminated, and the zero sequence is controlled to reduce oscillations in PNZSC strategy. The zero-sequence control has been less concern in the LVRT studies run on PV-connected grids. This control system reduces the oscillations in the AC and DC sides of the system. This fact increases the lifetime of PEIs and DC capacitors.

In general, in the proposed control strategy, the following issues are of concern:

1- Interleaved DC-DC converters, as well as Neutral Point Clamped (NPC) Inverter, are used to reduce THD and losses.

2- Amplifying of positive sequence current according to E.ON standard

3- Weakening and eliminating oscillations caused by the negative sequence current

4- Tackling zero-sequence current using proper switching technique in inverter.

5- A parallel braking resistor is employed in the DC-side, and a controller is designed to improve LVRT capability for two-stage grid-integrated PV systems.

3-1. Separating current sequences

In conventional SRF-frequency-locked loop (SRF_FLL), the voltage vector is transferred to the synchronous reference frame. The angle position for the dq reference frame is controlled through a feedback loop that set the q component to zero. This PLL is appropriate for balanced grids and in unbalanced grids, it is not easy to extract component d. In FLL, using a Dual Second Order Generalized Integrator (DSOGI_FLL) and applying some filters, the balanced signal elements are extracted, instantaneously. The DSOGI_FLL method is appropriate in three-phase systems applications and for high-level harmonics elimination. The output of DSOGI_FLL method enters the PNZSC Strategy. Also, an FLL is applied to provide a linear response for the frequency adaptation loop in DSOGI. This method makes it possible to estimate the symmetric components of the three-phase input voltage in the Cartesian $\alpha\beta$, separately [29].

3-2. Strengthening the positive sequence current through the E.ON standard and limiting the inverter output current to the maximum rated value

A short circuit fault in PV-connected grids leads to a voltage drop in the AC grid. In these circumstances, the current increases in the AC grid [30]. For compensation for the voltage drop caused by the fault, the grid allocates some parts of the injected power into the grid as reactive power, which disables PV operation in MPPT mode. As observed in Figure 3, the PV operation point is removed from the MPPT mode and is directed towards a new power generation point [21]. As shown in Figure 3, by moving the operating point, the voltage on the DC-side increases and the current on this side decreases**.**

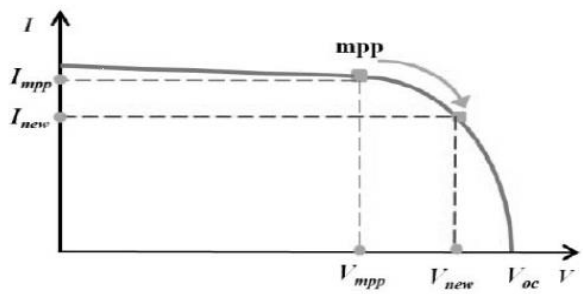


Figure 3. Change in PV operating point during AC voltage drop

3-3. Separating current sequences

For compensation for the voltage drop caused by the fault in the AC grid connected to the PV, reactive power is needed to be injected into the grid according to the E.ON standard, Eq. (2), [9]:

$$I^{*}_{q(pu)} = \begin{cases} 0 & V_{drop} < 0.1 \\ 2*V_{drop} & 0.1 < V_{drop} < 0.5 \\ 1 & V_{drop} > 0.5 \end{cases} \quad (2)$$

Parameter V_{drop} is calculated through Eq. (3):

$$V_{drop(pu)} = 1 - (|V_{rms}^{+}| / V_{base}) \quad (3)$$

where V_{base} equals the grid voltage. The $|V_{rms}^{+}|$ is calculated through:

$$|V_{rms}^{+}| = \sqrt{\frac{1}{3}(V_{pcca}^{+2} + V_{pccb}^{+2} + V_{pccc}^{+2})} \quad (4)$$

where the $V_{pcc(x)}$ is the voltage of the inverter to the grid point of common coupling (PCC), and (x) represents each phase; The PCC positive sequence voltage of each phase in unbalanced conditions is calculated from [15]:

$$\begin{bmatrix} V_{pcca}^{+} \\ V_{pccb}^{+} \\ V_{pccc}^{+} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}\begin{bmatrix} V_{pcca} \\ V_{pccb} \\ V_{pccc} \end{bmatrix} = \sqrt{2}|V_{rms}^{+}|\begin{bmatrix} \sin(\theta_i) \\ \sin(\theta_i - \frac{2\pi}{3}) \\ \sin(\theta_i + \frac{2\pi}{3}) \end{bmatrix} \quad (5)$$

where $a = e^{j2\pi/3}$.

3-3-1. Attenuation and elimination of oscillations due to negative-sequence current

In this process, the negative sequences are first separated by applying the DSOGI_FLL method, and next, the active and reactive powers are rewritten as [31]:

$$P = V.I = (V^{+} + V^{-} + V^{0}).(I^{+} + I^{-} + I^{0}) \quad (6)$$

$$Q = V_{\perp}.I = (V_{\perp}^{+} + V_{\perp}^{-} + V_{\perp}^{0}).(I_{\perp}^{+} + I_{\perp}^{-} + I_{\perp}^{0}) \quad (7)$$

where in both, V^{+} I^{-} ،I^{+} ،V^{0} ،V^{-} ،and I^{0} are the positive, negative, and zero sequences of voltage and the positive, negative, and zero sequences of grid currents, respectively. $V_{\perp}^{+}$ leads V^{+} with 90° and $V_{\perp}^{-}$ lags V^{+} with about 90°, and also $V_{\perp}^{0}$ equals zero. The dot product of the multiplications between I^{0} and the voltage vectors of the positive and negative sequences is always zero (due to the symmetry in V^{+} and V^{-} components); consequently, Eqs. (6 and 7) are rewritten as :

$$P = V.I = (V^{+} + V^{-}).(I^{+} + I^{-}) + (V^{0}.I^{0}) \quad (8)$$

$$Q = V_{\perp}.I = (V_{\perp}^{+} + V_{\perp}^{-}).(I_{\perp}^{+} + I_{\perp}^{-}) \quad (9)$$

where, as noticed, the zero-sequence leads to oscillation only at active power. To reduce the oscillations caused by the negative sequence, the apparent power should be rewritten in the static reference frame ($\alpha\beta$)[32].

$$S = \frac{3}{2}V_{\alpha\beta}.I_{\alpha\beta}^{*} = \frac{3}{2}\begin{bmatrix} V_{\alpha\beta}^{+} & V_{\alpha\beta}^{-} & V_{\alpha\beta}^{+} & V_{\alpha\beta}^{-} \end{bmatrix}\begin{bmatrix} I_{\alpha\beta}^{+*} \\ I_{\alpha\beta}^{+*} \\ I_{\alpha\beta}^{-*} \\ I_{\alpha\beta}^{-*} \end{bmatrix} \quad (10)$$

In the presented equations, the terms related to oscillations in apparent power are separated. Eq. (10) can be rewritten as follows [33]:

$$S = (P + P_{OSC}) + j(Q + Q_{OSC}) \quad (11)$$

where P_{OSC} and Q_{OSC} are the oscillation values of the active and reactive powers due to the negative sequence, respectively, calculated through Eqs. (12-15) [34]:

$$P = 3/2\begin{bmatrix} V_{\alpha}^{+} & V_{\beta}^{+} & V_{\alpha}^{-} & V_{\beta}^{-} \end{bmatrix}\begin{bmatrix} I_{\alpha}^{+} \\ I_{\beta}^{+} \\ I_{\alpha}^{-} \\ I_{\beta}^{-} \end{bmatrix} \quad (12)$$

$$P_{OSC} = 3/2\begin{bmatrix} V_{\alpha}^{+} & V_{\beta}^{+} & V_{\alpha}^{-} & V_{\beta}^{-} \end{bmatrix}\begin{bmatrix} I_{\alpha}^{-} \\ I_{\beta}^{-} \\ I_{\alpha}^{+} \\ I_{\beta}^{+} \end{bmatrix} \quad (13)$$

$$Q = 3/2\begin{bmatrix} V_{\alpha}^{+} & V_{\beta}^{+} & V_{\alpha}^{-} & V_{\beta}^{-} \end{bmatrix}\begin{bmatrix} I_{\alpha}^{+} \\ -I_{\beta}^{+} \\ I_{\alpha}^{-} \\ -I_{\beta}^{-} \end{bmatrix} \quad (14)$$

$$Q_{OSC} = 3/2\begin{bmatrix} V_{\alpha}^{+} & V_{\beta}^{+} & V_{\alpha}^{-} & V_{\beta}^{-} \end{bmatrix}\begin{bmatrix} I_{\alpha}^{-} \\ -I_{\beta}^{-} \\ I_{\alpha}^{+} \\ -I_{\beta}^{+} \end{bmatrix} \quad (15)$$

In the PNZSC strategy, the primary objective is to eliminate oscillations in the system. The active power is $P = P^{*}$, and the reactive power is $Q = Q^{*}$. The active reference power P^{*} and reactive reference power Q^{*} are calculated as:

$$P^{*} = |S|\sqrt{1 - I_{vr}^{*}} \quad (16)$$

$$Q^{*} = |S|I_{vr}^{*} \quad (17)$$

where I_{vr}^{*} is calculated through Eq. (2).

The active and reactive oscillating powers for oscillation elimination are defined as $P_{OSC}=0$ and $Q_{OSC}=0$, respectively. By setting the oscillating values of the active and reactive powers in the Eqs. (12-15) to zero, the reference currents are calculated as:

$$\begin{bmatrix} I_{\alpha}^{*}(wt) \\ I_{\beta}^{*}(wt) \\ I_{\alpha}^{*}(vr) \\ I_{\beta}^{*}(vr) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \frac{L_{wt}^{+}V_{\alpha}^{+}+L_{wt}^{-}V_{\alpha}^{-}}{A} & 0 & 0 & 0 \\ 0 & \frac{L_{wt}^{+}V_{\beta}^{+}+L_{wt}^{-}V_{\beta}^{-}}{A} & 0 & 0 \\ 0 & 0 & \frac{L_{vr}^{+}V_{\beta}^{+}+L_{vr}^{-}V_{\beta}^{-}}{B} & 0 \\ 0 & 0 & 0 & \frac{L_{vr}^{+}V_{\alpha}^{+}+L_{vr}^{-}V_{\alpha}^{-}}{B} \end{bmatrix} \begin{bmatrix} P^{*} \\ Q^{*} \\ P^{*} \\ Q^{*} \end{bmatrix} \quad (18)$$

where:

$$A = L_{wt}^{+}(V^{+})^{2} + L_{wt}^{-}(V^{-})^{2} \quad (19)$$

$$B = L_{vr}^{+}(V^{+})^{2} + L_{vr}^{-}(V^{-})^{2} \quad (20)$$

The L_{wt}^{+}, L_{wt}^{-}, L_{vr}^{+}, L_{vr}^{-} control coefficients are within [-1 1] range. The positive and negative voltage sequences are derived as:

$$V^{+} = \sqrt{(V_{\alpha}^{+})^{2} + (V_{\beta}^{+})^{2}} \quad (21)$$

$$V^{-} = \sqrt{(V_{\alpha}^{-})^{2} + (V_{\beta}^{-})^{2}} \quad (22)$$

where the current reference values are obtained by:

$$I_{\alpha}^{*} = I_{\alpha}^{*}(wt) + I_{\alpha}^{*}(vr) \quad (23)$$

$$I_{\beta}^{*} = I_{\beta}^{*}(wt) + I_{\beta}^{*}(vr) \quad (24)$$

In the equations for reference currents, the objective is to reduce the oscillations caused by the negative sequence. The control coefficients in Eq. (18) must be chosen so that the oscillating values of the active and reactive powers are reduced. According to the IEEE standard in [35], the VUF value should be less than 0.02:

$$VUF = V^{-}/V^{+} = \sqrt{(v_{\alpha}^{-})^{2} + (v_{\beta}^{-})^{2}} \Big/ \sqrt{(v_{\alpha}^{+})^{2} + (v_{\beta}^{+})^{2}} \quad (25)$$

Thus, according to Eq. (25), the control coefficients of the relations 18 must be such that this is achieved. Eqs. 23, 24, and 18 are inserted into (12-15), followed by selecting the control coefficients $L_{wt}^{+}=1$, $L_{wt}^{-}=-1$, $L_{vr}^{+}=0.5$ and $L_{vr}^{-}=0.5$ which eliminate the negative sequence caused by the active power completely, thus, $P=P^{*}$. At the Q, the oscillations are formed with twice the grid frequency, which reduces upon an increase in P^{*} and increases upon an increase in Q^{*}. Because the value of Q^{*} is zero during normal operating conditions and also at fault its value is negligible, the mean value of Q^{*} is small, and therefore oscillations are reduced in the grid.

The maximum apparent transferable power is calculated through Eq. (26) and $I_{\max} \le I_{rate}$. It always holds:

$$|S| = (|V_{pcca}|_{rms} + |V_{pccb}|_{rms} + |V_{pccc}|_{rms}) I_{\max} \quad (26)$$

By applying Eq. (18) in the synchronous reference, the circuit maximum tolerable passing current at a default time is calculated as follows:

$$I_{\max} = \sqrt{\frac{(V^{+})^{2} - 2V^{+}V^{-}\min(\Re) + (V^{-})^{2}}{(V^{+})^{2}} ((I_{p}^{+})^{2} + (I_{q}^{+})^{2})} \quad (27)$$

Parameters $\Re$ and I_p^{+} in Eq. (27) are:

$$\Re = (\cos(\varphi) \quad \cos(\varphi - \frac{2\pi}{3}) \quad \cos(\varphi + \frac{2\pi}{3})) \quad (28)$$

$$I_{p}^{+} = \frac{2}{3}(V^{+}/(V^{+})^{2} - (V^{-})^{2})P^{*} \quad (29)$$

Parameter I_q^{+} is calculated through Eq. 2.

3-3-2. The zero-sequence current control

In the system under study, the zero-sequence current flows through the ground interface between the NPC and the Wye-Grounded transformer. Here, due to the impedance inequality of the phases, the zero-sequence current is always flowing. Upon asymmetric fault occurrence in the grid, the zero-sequence current flow increases between the AC and DC parts of the system. This issue would reduce the NPC inverter input capacitor's durability and causes damage therein. It is necessary to apply some methods to reduce the oscillations caused by the zero sequence in the circuit to prevent this drawback. One of these methods is accomplished in this study by injecting the reference zero-sequence current and then addressing the zero-sequence in the inverter switching. As illustrated in Figure 4, the zero-sequence current flows between the DC and AC sides in the system, where i_N is the zero-sequence current flow through the ground on both sides of the system.

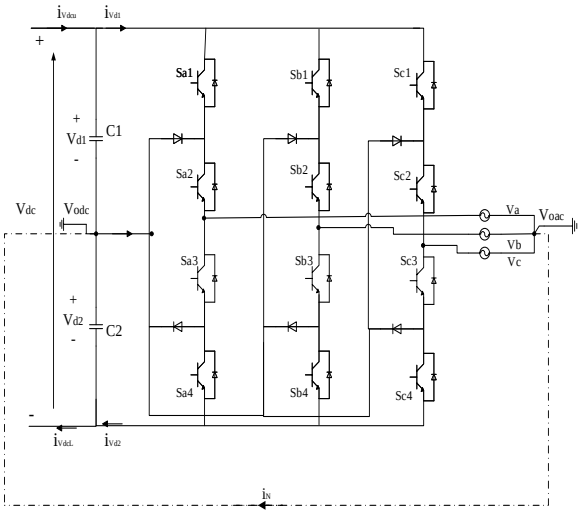


Figure 4. The zero-sequence current flow through the ground on both sides of the system drop

Table 1: Switching function

Switch	Status	Value
Sa1, Sa2	ON	**+1**
Sa2, Sa3	ON	**0**
Sa3, Sa4	ON	**-1**

The switching functions of the inverter are tabulated in Table 1, in which if two switches are ON, the others remain OFF.

As the capacitances C_1 and C_2 of the system shown in Figure 4, are equal, then $i_{vdcu} = -i_{vdcL}$.

The following equations are held for the top and bottom capacitors at the inverter input [36]:

$$C_1 dV_{d1}/dt = i_{vdcu} - i_{vd1} \quad (30)$$

$$C_2 dV_{d2}/dt = i_{vdcL} - i_{vd2} \quad (31)$$

that is:

$$C\, d(V_{d1} - V_{d2})/dt = i_N \quad (32)$$

where $C_1 = C_2 = C$.

Eq. (32) is rewritten as:

$$C\, d(V_{d1} - V_{d2})/dt = 3i_0 \quad (33)$$

where the i_0 is equal to zero-sequence current.

Currents i_{vd1} and i_{vd1} are calculated from Equations (34) and (35). In these equations, the status of the switches in each phase is represented by $K_{a\ or\ b\ or\ c}$, where a, b, and c represent the intended phase [19, 36].

$$i_{vd1} = 0.5[K_a(t)+1]i_a(t) + 0.5[K_b(t)+1]i_b(t) + 0.5[K_c(t)+1]i_c(t) \quad (34)$$

$$i_{vd2} = 0.5[K_a(t)-1]i_a(t) + 0.5[K_b(t)-1]i_b(t) + 0.5[K_c(t)-1]i_c(t) \quad (35)$$

The currents i_{vd1} and i_{vd2} can be rewritten as Eqs. (36 and 37) based on the total of the zero-sequence current and the DC side current.

$$i_{vd1} = i_{chop} + 0.5i_N \quad (36)$$

$$i_{vd2} = i_{chop} - 0.5i_N \quad (37)$$

where the values i_{chop} and i_N are defined through Eqs. (38 and 39):

$$i_{chop} = 0.5[K_a i_a + K_b i_b + K_c i_c] \quad (38)$$

$$i_N = i_a + i_b + i_c \quad (39)$$

in which, i_{chop} is equal to the chopper output current and the entry to the inverter in the DC side.

In order to control the zero sequence when switching the inverter, the zero sequence is no longer considered a constant value of zero. By comparing the reference value of zero sequences caused by the voltage difference between the upper and lower capacitors and the zero-sequence current flowing within the DC and AC sides of the system, this value is considered the zero input sequence current for the switching.

In general, according to the amplitude modulation coefficient of each phase $m_i(t)$ and the switching function value tabulated in Table 1, the DC-side current can be rewritten as [19]:

$$\sum_{i=a}^{c} \frac{1}{2}[m_i(t).I_i(t)] = \frac{1}{2}\sum_{i=a}^{c}[m_i(t)].[I_{iwz}(t) + I_{iz}(t)] = \frac{1}{2}\sum_{i=a}^{c}[m_i(t).I_{iwz}(t)] + \frac{3}{2}(m_i(t).I_{iz}(t)) \quad (40)$$

Here, i represents each phase, $I_{iwz}(t)$ is the sum of each phase's positive and negative sequence currents, and $I_{iz}(t)$ is the zero-sequence current. If the phase impedances are equal and the fault is symmetric, the zero-sequence will not flow in the circuit; otherwise, the zero-sequence value is calculated through Eq. (39). The amplitude modulation $m_i(t)$ is calculated by Eq. (41), which leads to the formation of a second harmonic expression $m_i(t).I_{iz}(t)$ in the circuit, resulting the oscillation. Injection of zero-sequence currents upon switching reduces the $m_i(t).I_{iz}(t)$, thus, a reduction in circuit oscillations.

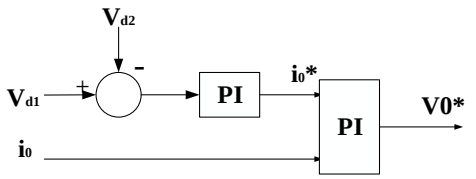


Figure 5. Zero sequence injection for the inverter switching

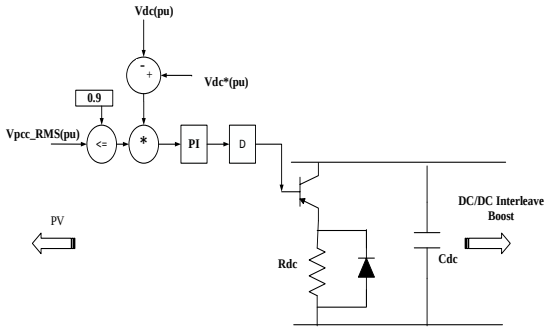


Figure 6. Braking resistor on the DC side

Table 2: The PV specifications

Parameter	Value
Number of Parallel String	1
Number of series modules	10
Maximum Power (W)	210W
Open circuit voltage Voc (V)	40W
Short-circuit current Isc (A)	8A

Table 3: System specifications (figure 7a)

Parameter	Value
Generated active power	1.7kW
Grid line-Line voltage (RMS)	190V
Nominal grid frequency	50HZ
Rated current amplitude	4.5A
Inverter side inductance of the LCL filter	1.6mH
Grid side inductance of the LCL filter	26.1mH
The capacitance of the LCL filter	2.6μF
dc-link capacitor (two in series)	3760μF
Sampling/Switching frequency	20kHZ
The impedance of phase a	(1.87921+8.532j)Ω
The impedance of phase b	(1.8584+8.2242)Ω
The impedance of phase c	(1.9032+7.9189)Ω

$$m_i(t) = V_{control} / V_{tri} \quad (41)$$

Here, $V_{control}$ is the control signal at zero sequences, and V_{tri} is the triangular waveform of the SPWM switching method.

Figure 5 shows zero-sequence injection for the inverter switching, in which V_{d1} and V_{d2} are the capacitor voltages inverter inputs.

3-3-3. Employing a braking resistor on the DC side

Upon a fault occurrence, the capacitor voltage on the DC side moves towards the open circuit mode leading to a current decrease on the DC side and an increase in its voltage [21]. This phenomenon necessitates the DC-link voltage control to improve LVRT conditions. In normal conditions, the power of the PV array is furnished to the grid through a capacitor on the DC side. The grid codes determine the reference reactive power during LVRT. The active power injected into the grid must be subject to the reference power. The power imbalance in the system occurs when there is an inequality between the reference power and the injected active power. This issue usually appears upon an unbalanced voltage drop; because most of the inverter capacity is usually occupied as the injected reactive power. Thus, it does not allow to preserve the maximum injected active power from the PV array to the grid. To overcome this drawback, the PV is put in NOT MPPT mode, which reduces active power injection by the inverter. If the PV is still in the MPPT mode, the power imbalance may increase the DC-link capacitor voltage, damaging the capacitor and shortening its lifespan. A constant DC-link voltage must be generated to protect the DC-link capacitor against overvoltage. According to [37], this can be achieved by reducing the power of the PV array by replacing the operation point from the MPP in the P-V curve with the new operation point and reducing the reference power [37]. A braking resistor is used on the DC-side, to prevent the increase in the voltage and then protecting the inverter upon a fault [38]. Figure 6 shows how the DC resistor is added to the circuit upon a fault. The parallel resistance value is computed as [39]:

$$R_{dc} = V_{dc}^2 / P_{dc} \quad (42)$$

3-3-4. The block diagram of the system

The understudied system contains a PV with the specifications tabulated in Table 2. This system supplies power to a $2KW$ three-phase grid with $V_{rms} = 190V$ voltage and $50HZ$ frequency. The employed two-stage PEI includes a DC/DC interleaved boost converter and an NPC inverter. The system specifications of Figure 7a are presented in Table 3.

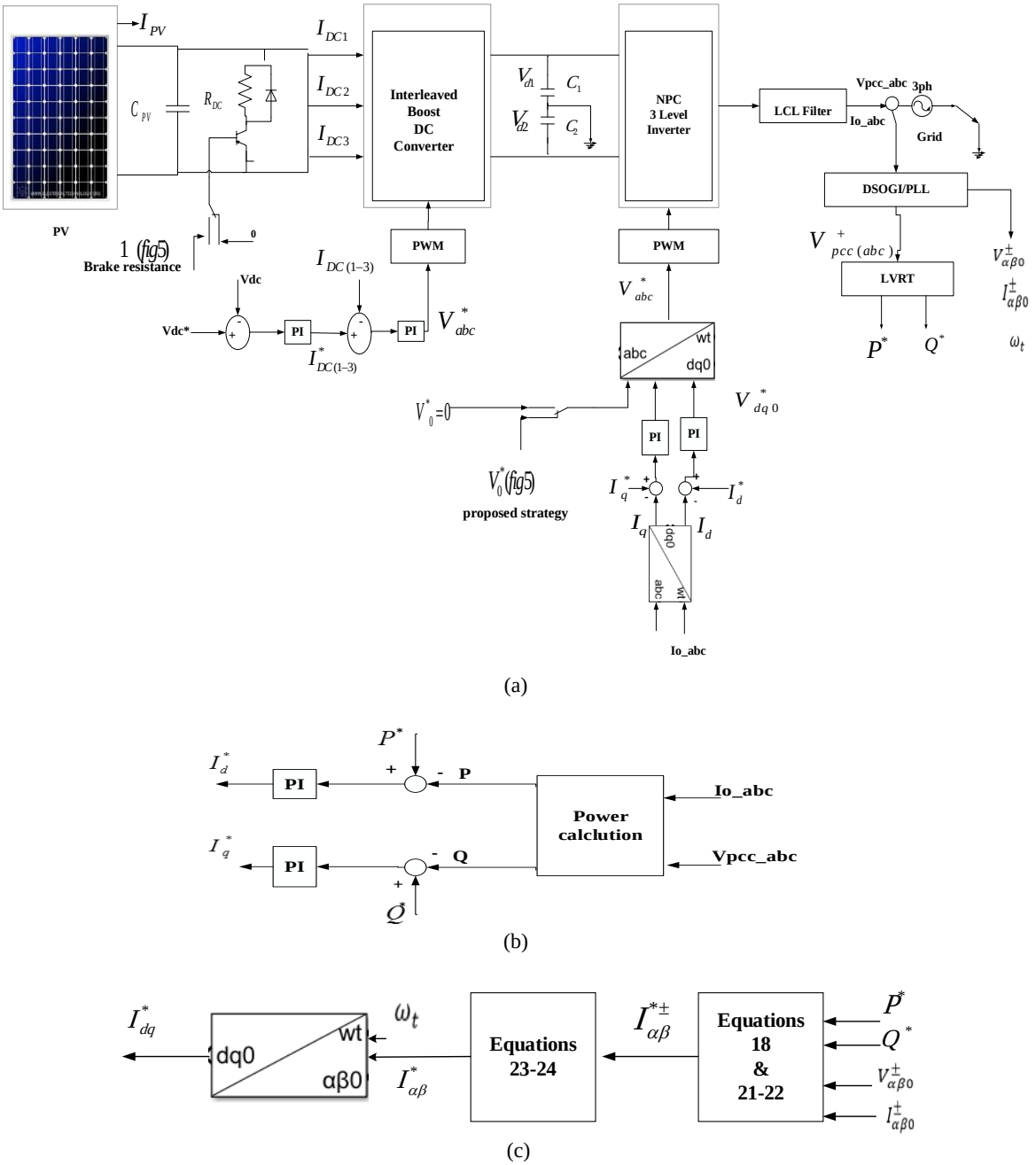


Fig.7. The block diagram of the system, a) the system connected to PV contains an NPC inverter and three-level Interleaved Boost DC / DC converter b) Conventional LVRT strategy c) This proposed LVRT strategy.

4. Simulation results

The simulations are performed in MATLAB/Simulink software environment. The proposed control approach shown in Figure 7c, is compared with the method shown in Figure 7b, to reveal the outperformance of c vs. b.

Simulations are carried out in three scenarios: 1) a three-phase fault with duration of *150ms* on the grid side, where the inverter output voltage drops from *1*

pu to *0.3 pu*, 2) a single-phase to ground fault with the same duration and 3) a two-phase fault with the same duration.

Two modes are of concern in comparing the simulation results in each case: 1) The negative sequence, due to system imbalance and the asymmetric fault is not eliminated. In this case, through the control strategy, the inverter is switched by the SPWM method and zero sequence is not injected, that is, the values $I_0^* = 0$ and $I_0 = 0$. Here, the control is without the proposed strategy and only with the PI controller, in which the proportional coefficient *(P)* equals *0.01*, and the integral coefficient *(I)* equals *0.5* (shown in Figure 7b) 2) The proposed control strategy eliminates the negative sequence due to system imbalance and asymmetric faults. Here, the inverter is switched by the SPWM method, and zero sequences are injected; that is, the I_0^* is calculated according to Figure 5 and I_0 is equal to the zero-sequence current value in the circuit (shown in Figure 7c).

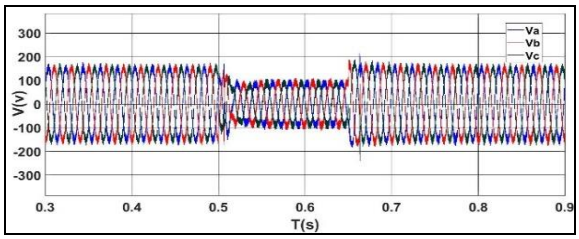
The simulation results are shown in Figures 8–13 and the assessed results are tabulated in Table 4.

As observed in Figures 8a, 9a, 8b and 9b, upon fault occurrence and elimination, the sudden increases in voltage and current are higher, compared with the conventional control method. In this case, the fault is symmetric. Due to the imbalance state of the grid, negative and zero-sequence currents cause oscillation in the circuit. In Figure 8c, the voltage oscillation is greater than the proposed approach. Also, Figure 8d shows higher active power injection into the grid than the proposed approach. The most important part of the proposed zero-sequence control strategy is shown in Figure 8e. The lack of control in zero-sequence current leads to a voltage difference between the two inverter input capacitors. According to Eq. (33), this voltage difference makes the current flow between the common ground of DC side and the Wye-grounded transformer grid. This current causes oscillations in the grid-connected solar power plant**.**

As observed in Figures 10a, 11a, 10b and 11b, upon fault occurrence and elimination, the sudden increase in voltage and current surge are higher when the conventional control method is employed. The current jump is about 4 amps less when the proposed strategy is used. In this case, due to the asymmetric single-phase fault occurrence in the ground, there is the negative and zero-sequences flow in the circuit, compared with the former case. In Figure 10c, the voltage oscillation is greater than the proposed method upon fault occurrence. As observed in Figure 10d, this increases the active power injection into the grid. Oscillations of the active and reactive powers are remarkable when the conventional method is employed. The essential part of the proposed zero-sequence control approach, as shown in Figure 10e, is the lack of control on the zero-sequence current that leads to a voltage difference between the two input capacitors. According to Eq. 33, this voltage difference leads to current flow between the common ground of the DC side and the grid Wye-grounded transformer. This current causes oscillations in the grid-connected solar power plant**.**

Table 4: The results of the conventional and the proposed methods

Controller / Result	conventional strategy			Proposed strategy		
	Case1	**Case2**	**Case3**	**Case1**	**Case2**	Case3
$\Delta I_{\max} = I_{\max} - I_{Rate}(A)$	5	24	11	4	20	**13**
$THD(\%)$	66.26	64.28	22.13	4.7	4.12	**4.98**
$\Delta V_{RMS} = V_{\max} - V_{\mathrm{Re}f}(V)$	85	40	55	72	35	**57**
$\Delta P = P_{\mathrm{Re}f} - P_{injection}(W)$	262	210	223	20	0	**10**
$\Delta V_{dc} = V_{d1} - V_{d2}(V)$	2	26	16	0	16	**1**



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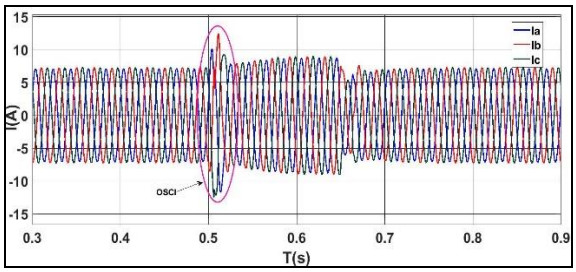

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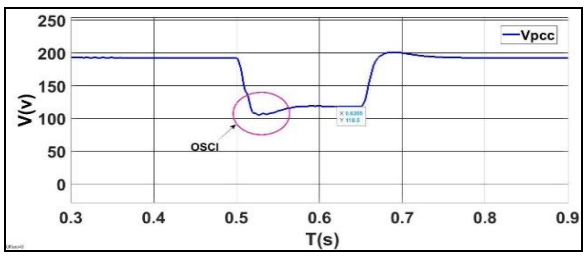

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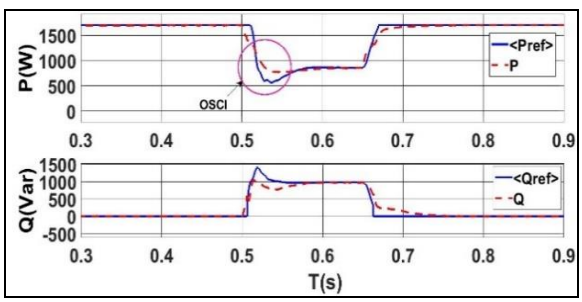

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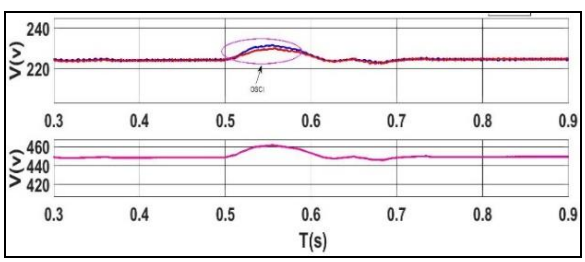
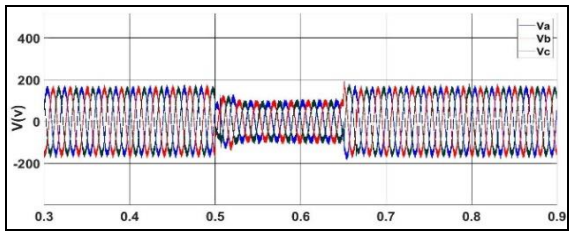


e

Figure 8: Simulation results of the case with a conventional approach: a) PCC voltage b) PCC current c) rms voltage in PCC d) active and reactive power of the grid e) voltage of the DC side



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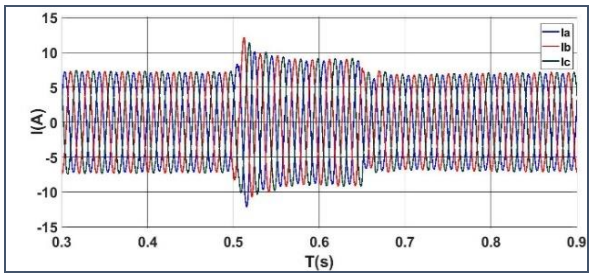

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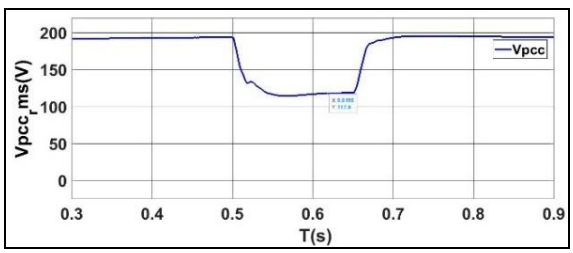

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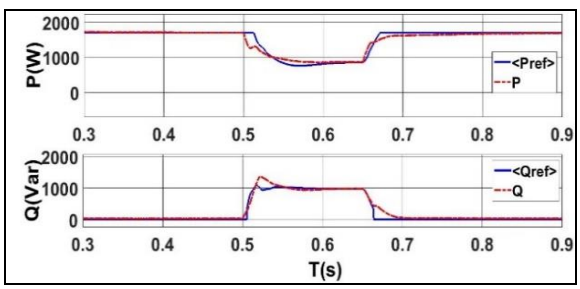

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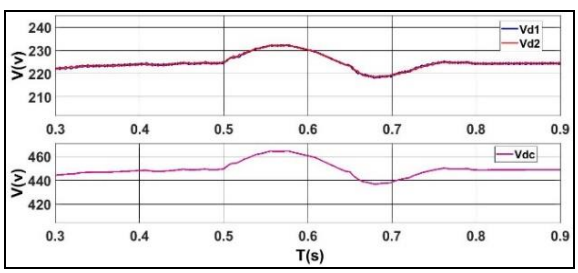

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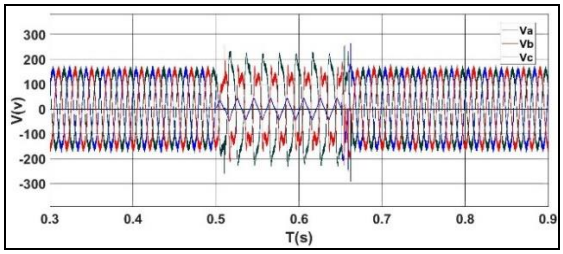
Figure 9: Simulation results of the case with the proposed approach: a) PCC voltage b) PCC current c) rms voltage in PCC d) active and reactive powers of the grid e) voltage of the DC side



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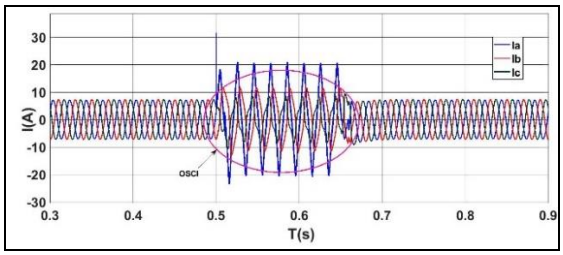

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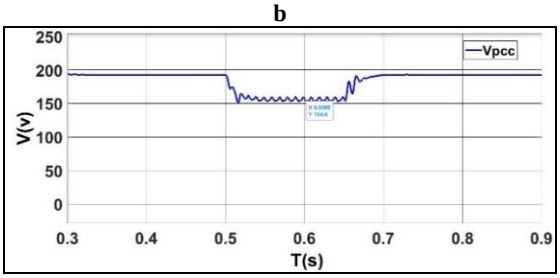

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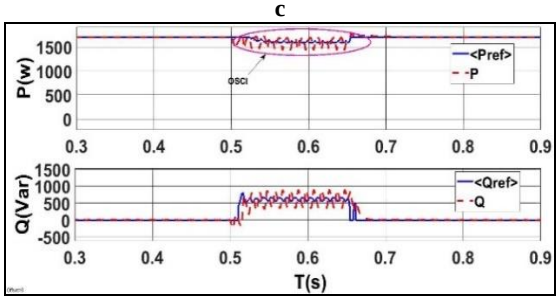

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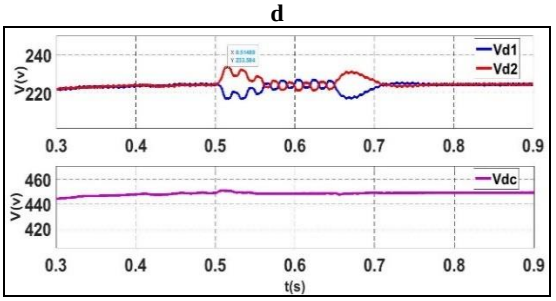

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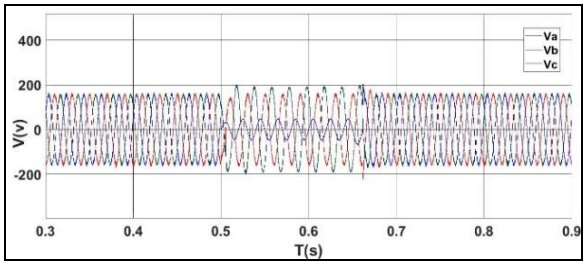
Figure 10: Simulation results of case two with a conventional strategy: a) pcc voltage b) pcc current c) rms voltage in pcc d) active and reactive power of the grid e) inverter voltage input capacitors on the DC side



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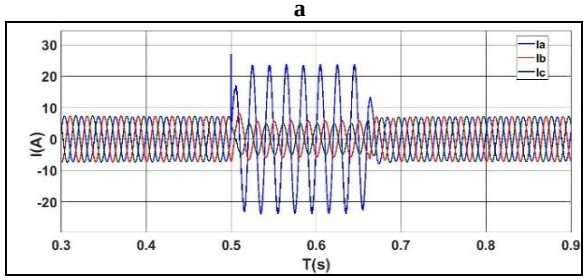

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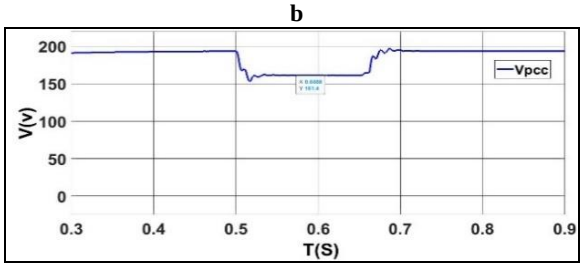

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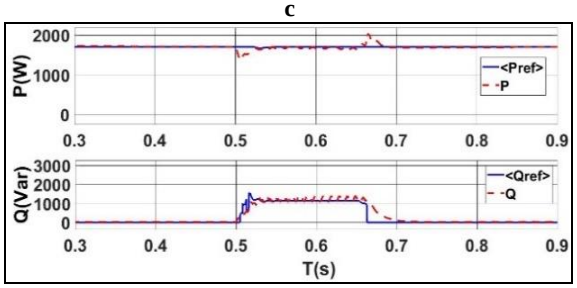

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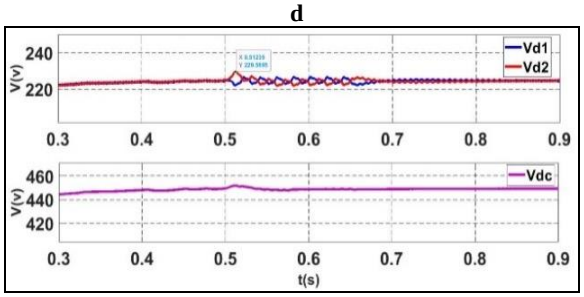

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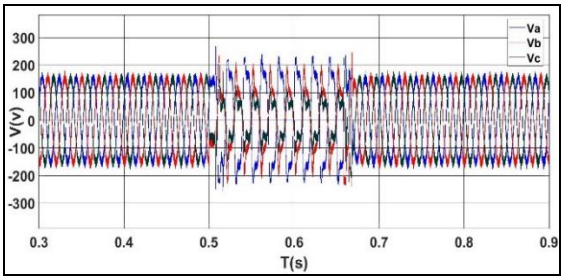
Figure 11: Simulation results of case two with a proposed strategy: a) pcc voltage b) pcc current c) rms voltage in pcc d) active and reactive power of the grid e) inverter voltage input capacitors on DC side



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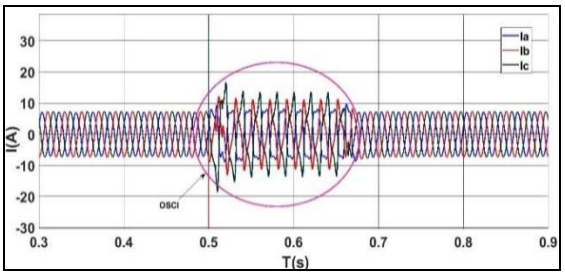

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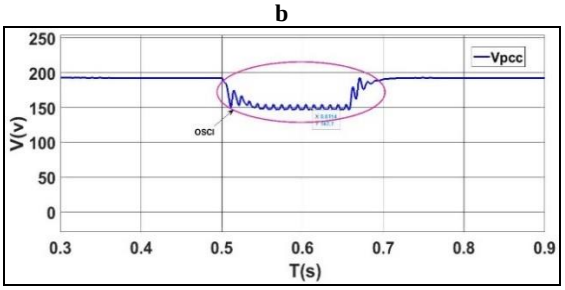

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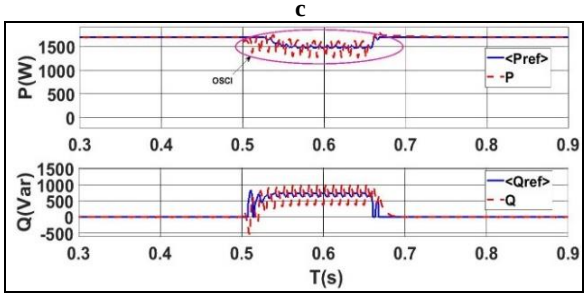

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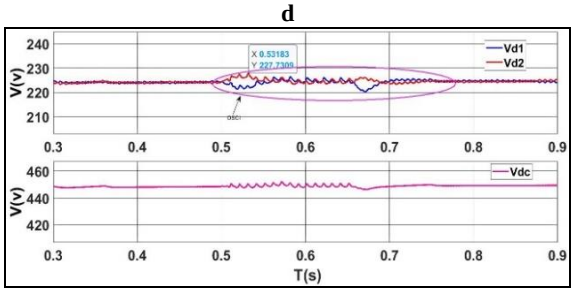

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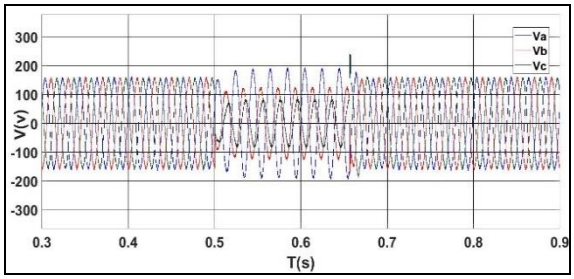
Figure 12: Simulation of the results of case three with a conventional strategy: a) PCC voltage b) PCC current c) rms voltage in PCC d) active and reactive power of the grid e) inverter voltage input capacitors on the DC side



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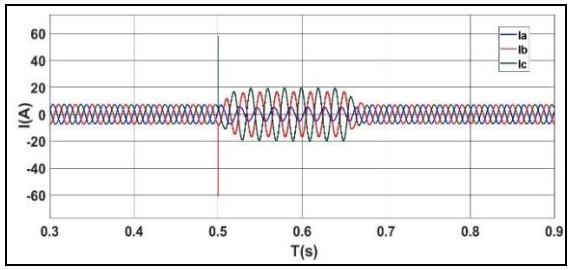

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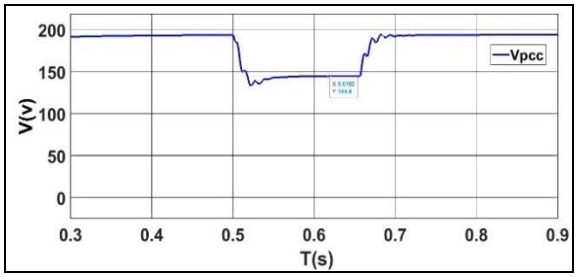

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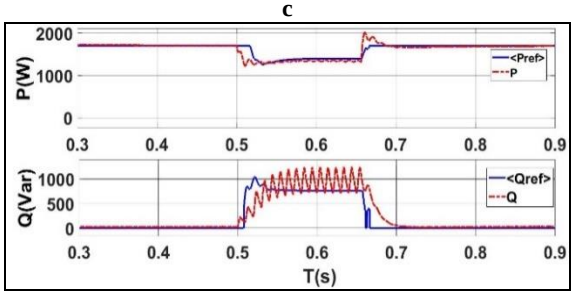

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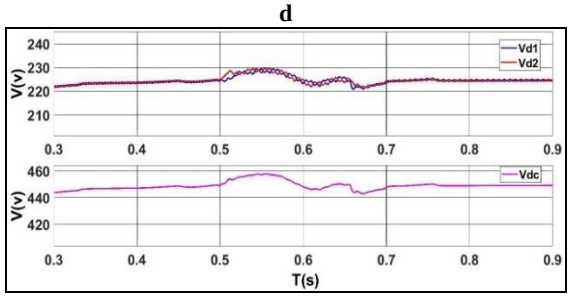

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Figure 13: Simulation of the results of case three with a proposed strategy: a) PCC voltage b) PCC current c) rms voltage in pcc d) active and reactive power of the grid e) inverter voltage input capacitors on DC side

Table 5: Comparison of the maximum voltage of DC side in case of single-phase fault occurrence to the ground with and without the braking resistance

Result / Controller	without braking resistance	With braking Resistance
V_{d1} &$V_{d2}(V)$	240.23	227.3
$V_{dc}(V)$	480.18	456.9

Table 6: PI Parameter

Kp(P)	Ki(P)	Kp(Q)	Ki(Q)	Kp(Z)	Ki(Z)
0.17	1.64	0.3	1.33	0.76	1.4

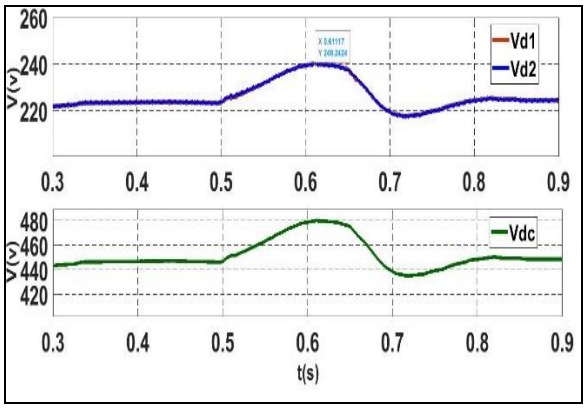


Figure 14: DC side voltage of each capacitor, without the braking resistance

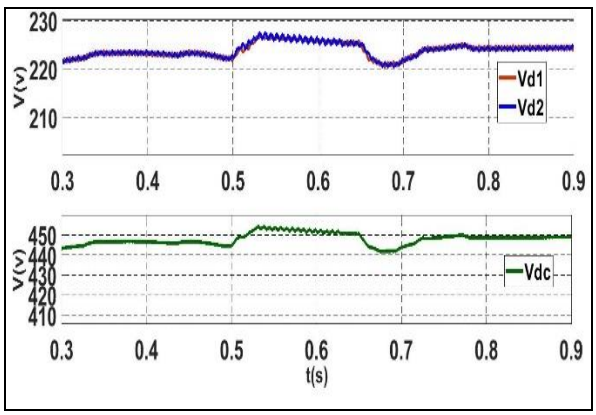


Figure 15: DC side voltage of each capacitor, with the braking resistance

As observed in Figures (12a and 13a) and (12b and 13b), sudden surges in voltage and current are inevitable when the conventional control method is employed. At the same time, the asymmetric two-phases fault generates a considerable value of negative and zero sequences in the circuit. The voltage oscillation is greater than the proposed approach, as shown in Figure 12c. This increases the oscillation of the active and reactive powers injected into the grid, as shown in Figure 12d. As shown in Figure 12e, the lack of control over zero-sequence current leads to a voltage difference between the two input capacitors. According to Eq. (33), this voltage difference leads to current flow between the common ground of the DC-side and the grid Wye-grounded transformer. This current causes oscillations in the grid-connected solar power plant.

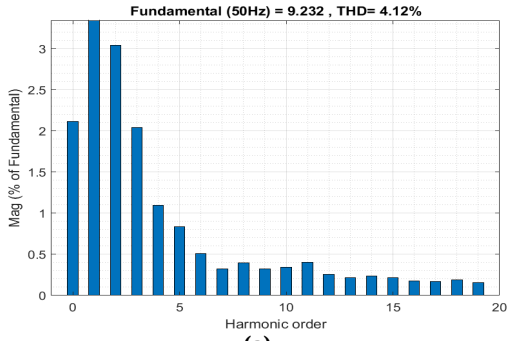
The simulation results obtained from the conventional and proposed approaches are tabulated in Table 4.

Now, the impact of braking resistance placed at the DC-side is investigated. Figure 14 shows the DC-side voltage value at a single-phase fault to ground, when the braking resistance is not parallel with the chopper. The same is observed in Figure 15 with the braking resistance. It is revealed that when the braking resistance becomes parallel with the DC/DC converter at fault occurrence, the overvoltage caused by the fault on the DC side decreases. This reduction prevents damage to the semiconductor components. This also increases the lifetime of the DC side capacitors. The V_{d1} and V_{d2} are the voltage values of each capacitor before the three-level NPC inverter, and V_{dc} is the voltage of the larger capacitor at the end of the boost converter. The simulation results with and without using the braking resistance are tabulated in Table 5.

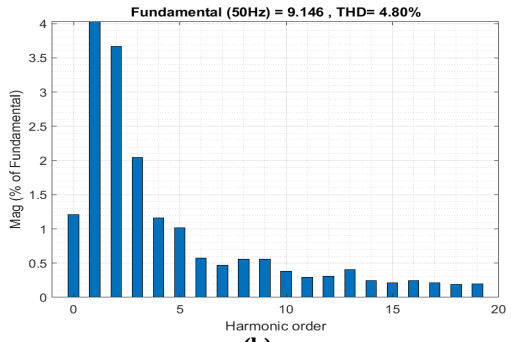
Also, Table 6 presents the coefficients of PI controllers.

3-4. Validation

In addition to the positive and negative sequences, the zero sequence has also been taken into account in the proposed method and the corresponding amount of THD is equal to 4.12% (Figure 16a), while in [15] and [40], in which the zero sequence has been ignored, the values of THD are equal to 4.8% (shown in Figure 16b) and 8.3%, respectively.



(a)



(b)

Figure 16: THD, a) PNZSC method. b) PNSC method [15].

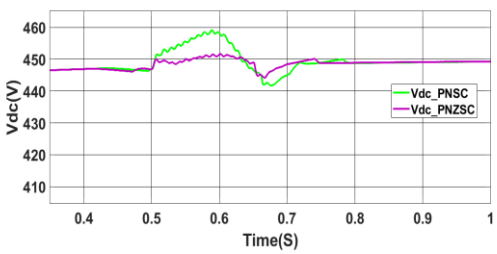


Figure 17: DC side voltage

Another feature of the simultaneous control of the three sequences, is the reduction of oscillations in the DC side. The performance of the proposed method of PNZSC is better than the one of the PNSC method employed in [40], as shown in Figure 17.

Also, Figures 18 and 19 show the voltage at the PCC point and the active power injected into the grid, respectively, for the proposed PNZSC method and the PNSC method presented in [40]. It is seen that the voltage of the PCC point has a lower drop during the fault using the proposed method and, correspondingly, the resultant value of active power also oscillates less than the PNSC method.

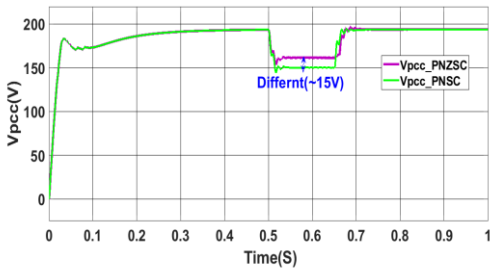


Figure 18: PCC point voltage

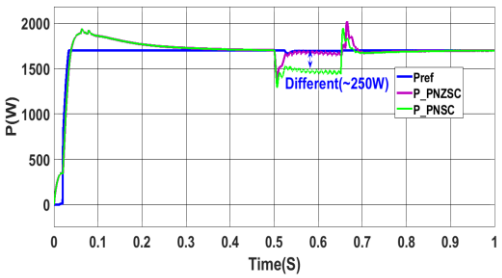


Figure 19: active power injected into the grid

4. Conclusions

This article was aimed to improve LVRT capability of the grid-connected PV farm in unbalanced AC grid conditions. By employing the DSOGI-FLL, first, the sequences are separated. Then, according to the PNZSC strategy, the positive sequence is increased, the negative sequences is eliminated, and the zero sequence is also addressed in the inverter switching template. This strategy reduces the THD value to a certain degree. Upon a fault occurrence, reactive power is injected to the grid according to the E.ON standard and the inverter output current is limited to the maximum rated value. During the fault in the AC grid, the voltage in the DC side rises abruptly, which can damage the semiconductor components and reduces lifespan of the DC side capacitors. For this purpose, a parallel braking resistor is used on the chopper and inverter path. In this case, there would be about 5% reduction in the DC side voltage during fault. The performance of the proposed approach is compared with a conventional method by simulating different possible scenarios. The results confirm the superiorities of the proposed method from different aspects. For future studies, non-linear controllers and intelligent algorithms can be designed and employed to have a real-time adaptation for PI controller coefficients to overcome disturbances.

Nomenclature

LVRT	Low Voltage Ride Through
DSOGI_FLL	Dual second Order Generalized Integrator - Frequency Locked Loop
NPC	Neutral Point Clamped
PEI	Power electronic interfaces
SRF	Synchronous reference frame
VUF	Voltage unbalance force
MPPT	Maximum Power Point Tracking
PV	Photovoltaic
THD	Total Harmonic Distortion
δ	DC / DC converter duty cycle
PCC	Point of Common Coupling
$V_{pcc(x)}$	the voltage of the inverter to the PCC(V)
P_{OSC}	the oscillation values of the active power (W)
Q_{OSC}	he oscillation values of the reactive power (var)
$I_{\max}$	The circuit maximum tolerable passing current (A)
P^*	The active reference power(W)
Q^*	The reactive reference power(var)
$I_{iwz}(t)$	The sum of each phase's positive and negative sequence currents(A)
$I_{iz}(t)$	The zero-sequence current (A)
$V_{control}$	The control signal at zero sequences(V)
V_{tri}	The triangular waveform(V)
V^+	Positive sequence voltage (V)
V^-	Negative sequence voltage (V)
V^0	Zero sequence voltage (V)
I^+	Positive sequence current (A)
I^-	Negative sequence current (A
I^0	Zero sequence current (A)

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